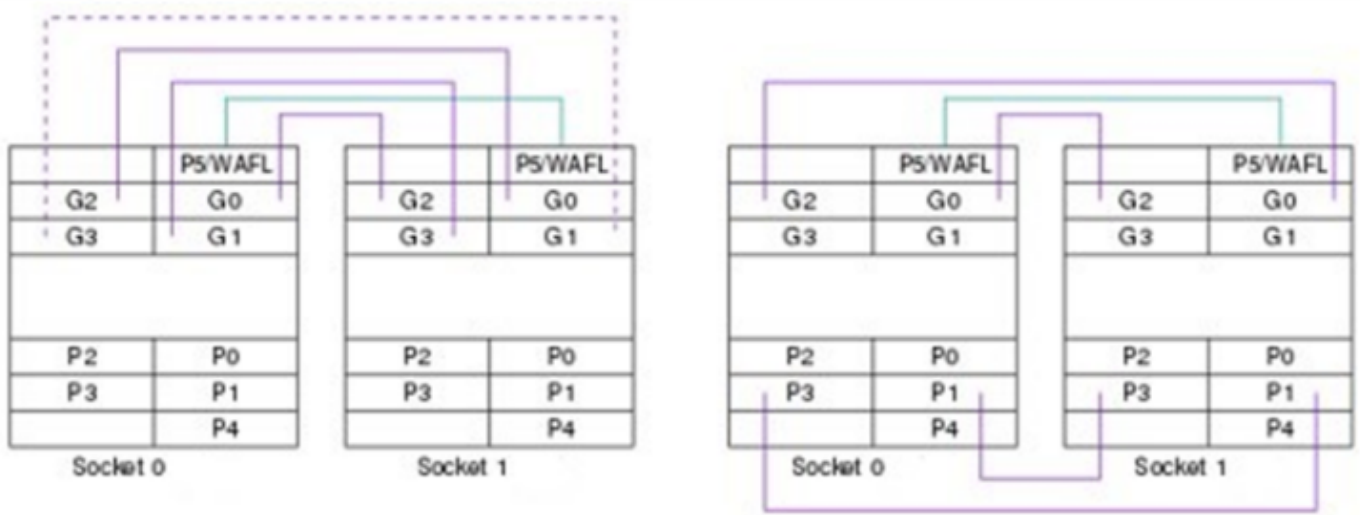
EPYC processor features and specifications

Features and technical specifications

Lenovo

Zen4 SP5 architecture

- Socket SP5 supports eight 16-lane multi-function I/O interfaces, P0-P3 and G0-G3. All of these interfaces can be configured as PCIe links. Alternatively, some lanes can be configured as xGMI links and other lanes as CXL or SATA links.
- On dual socket (2P) systems, the cache coherent xGMI links connect the Data Fabrics of each processor. SP5 processors can use three or four xGMI links depending on bandwidth requirements using the G0-G3 interfaces, or four links between G0, G2, P1, and P3. xGMI links use 16 lanes, and unused links release 16 lanes per socket for I/O. As with PCIe links, the maximum raw data rate is 32 GT/s.
- A Wide Area Functional Link (WAFL) connects the Control Fabrics of each processor for temperature monitoring and power and frequency control. Physically, they use the PCIe 3.0 protocol.

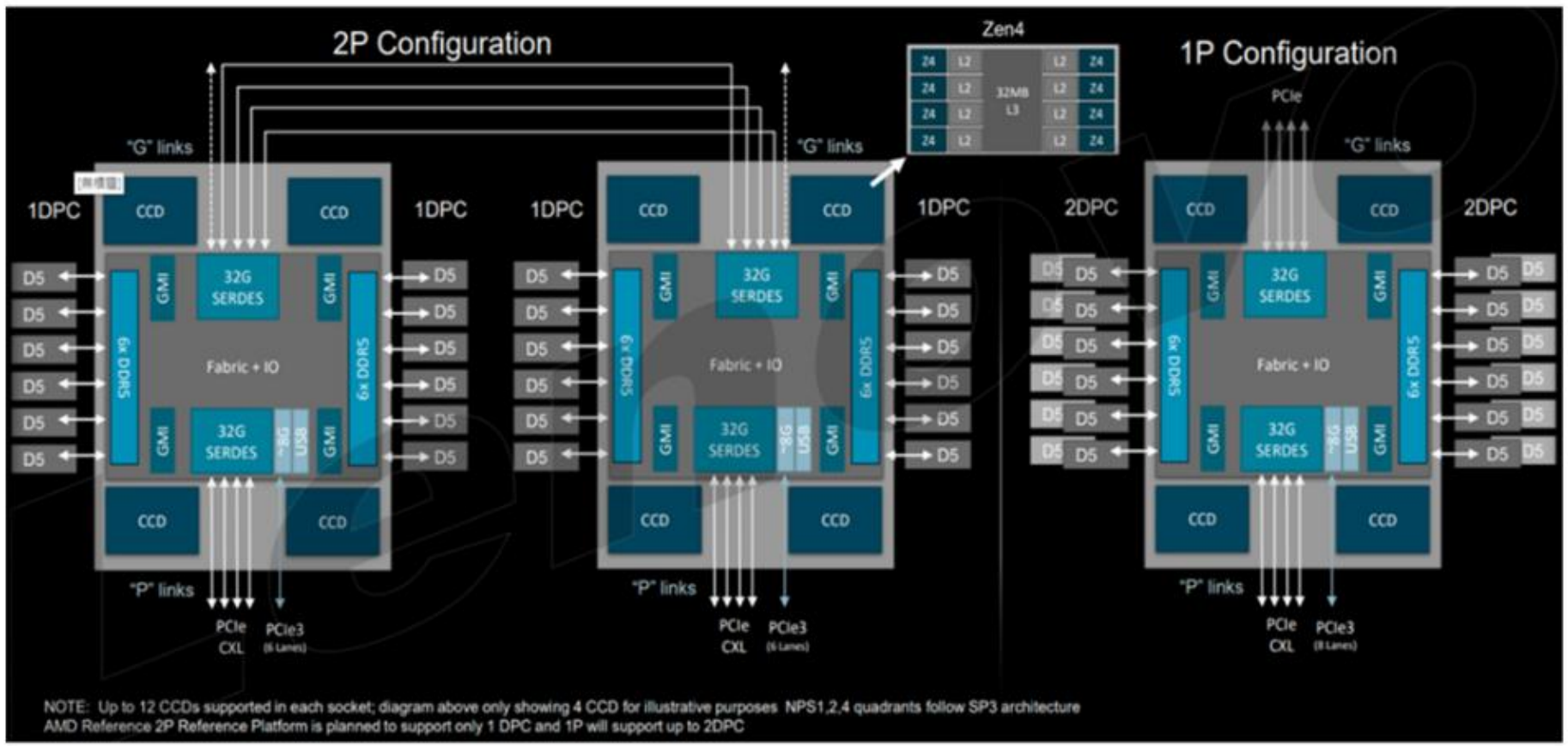


EPYC SP5 platform processor specifications

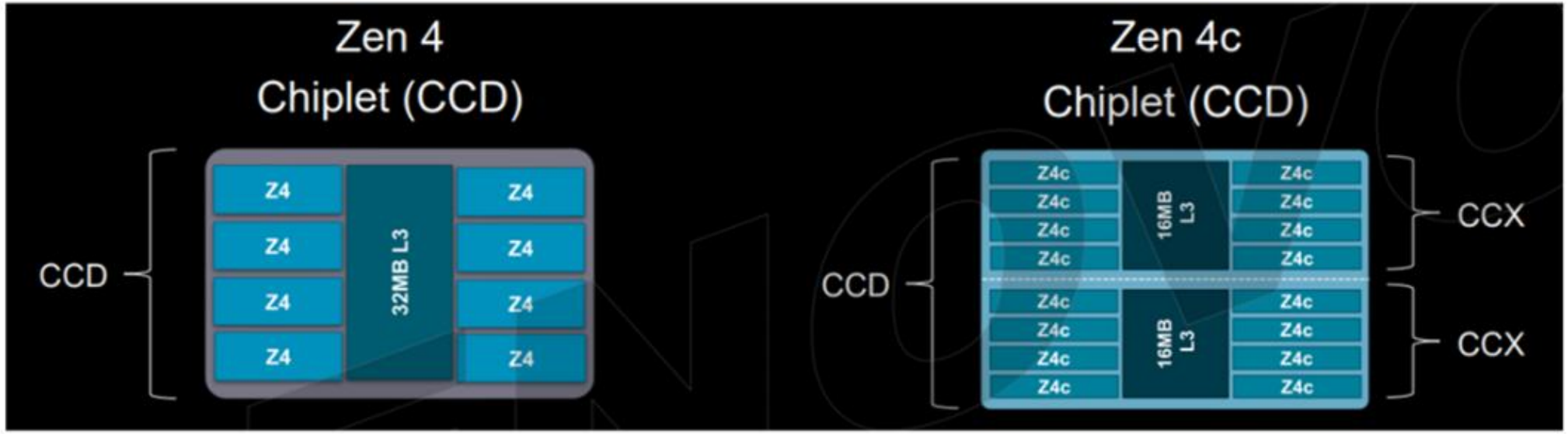
Feature	Specifications
Package type	LGA
Dimensions (mm)	72.0 x 75.4
Pins	6096
Pin pitch (mm)	0.94 x 0.81
CPU supported	Genoa SP5, Bergamo SP5, Turin SP5
Socket	Heat sink actuated SM-LGA socket
TDP	200 to 400 W
Memory configuration	12 DDR5 4800 MHz channels, 1/2 DPC
PCIe configuration	• PCIe 5.0, 128 lanes per socket • 128 to 160 lanes on a 2P node – Bonus 8 PCIe 3.0 lanes, 4 lanes per socket • 12 lanes in a 2P configuration • 32 SATA lanes per socket on P0/G3
CXL1.1+ configuration	64 lanes on P links configured for CXL1.1+
xGMI (Socket to Socket)	3 to 4 links, 3rd Gen Infinity up to 32 Gbps
I/O and xGMI configuration	New topology support added – front and rear I/O
DIMM types	RDIMM, 3DS RDIMM

Zen4 SP5 architecture block diagram

- Two-socket configurations are connected via three or four xGMI (“G” links). The “P” links support PCIe CXL.
- The two-processor configuration supports one DIMM per channel, and the one-processor configuration supports two DIMMs per channel.



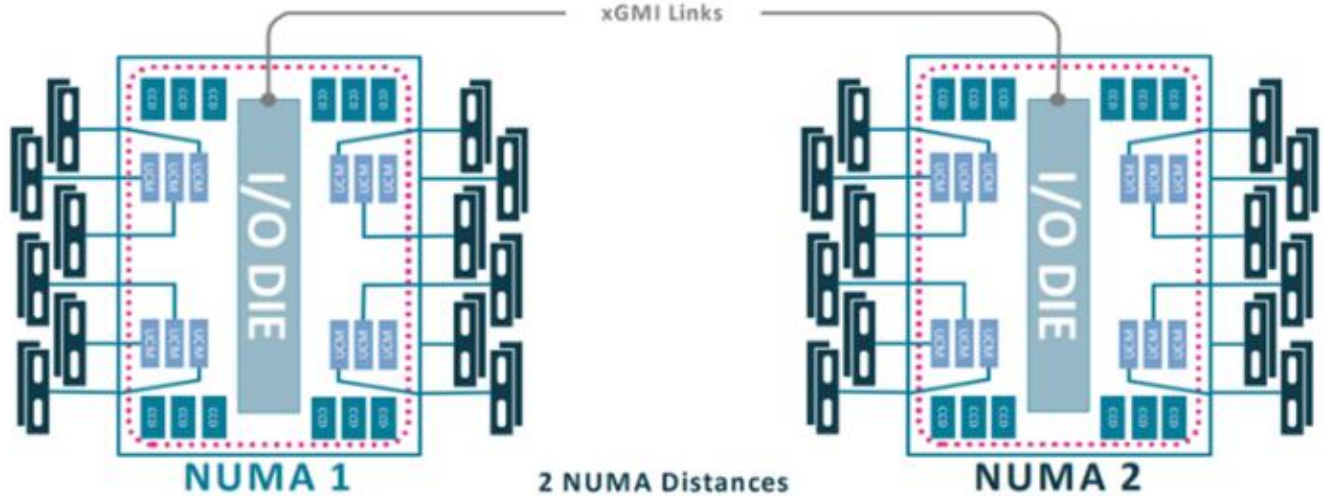
EPYC Zen4 chiplets



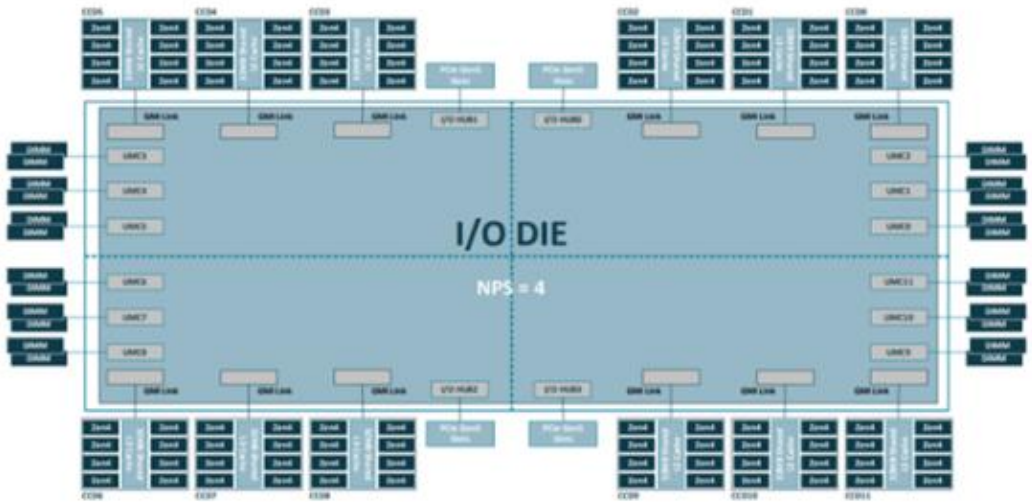
- Similar architecture to Milan
- Optimized for performance per core
- 1 MB of L2 cache per core
- 32 MB of shared L3 cache per CCD

- Dense core design
- Optimized for performance per watt
- 1 MB of L2 cache per core
- 16 MB of shared L3 cache per CCX (Core Complex)
- 32 MB of shared L3 cache per CCD

NUMA nodes per socket (NPS)



Two EPYC 9004 Processors connect through 4 xGMI links (NPS1)



- A two-socket system has a total of 24 memory channels, or 12 per socket. Two-socket systems can be configured in a variety of ways, including with 1, 2, 4, 8, or 24 NUMA nodes.
- “L3AsNumaNode” depends on the CPU SKU.

EPYC platform specification comparisons

Scroll down for more information

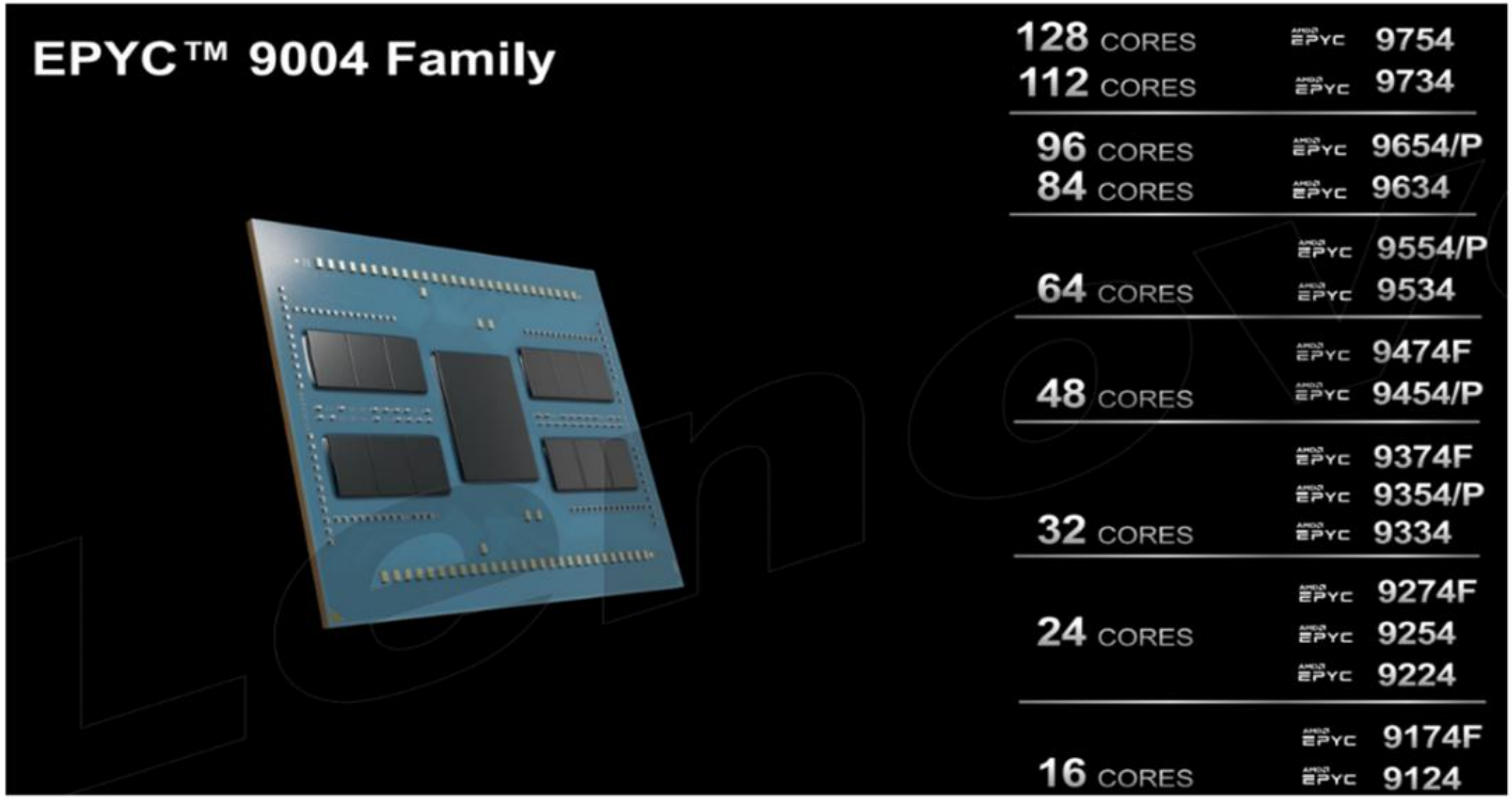
Platform	SP3	SP5	SP6
Package Type	LGA	LGA	LGA
Dimensions (mm)	58.5 x 75.4	72.0 x 75.4	58.5 x 75.4
Pins	4094	6096	4844
Pin pitch (mm)	1.00 x 0.87	0.94 x 0.81	0.94 x 0.81
CPUs supported	Naples, Rome, Milan	Genoa SP5, Bergamo SP5, Turin SP5	SIENA SP6, SORANO SP6
Socket	SAM actuated SM-LGA socket	Heat sink actuated SM-LGA socket	Hybrid actuated SM-LGA socket
TDP	120 to 280 W	200 to 400 W	70 to 225 W
Memory configuration	Eight DDR4 3200 MHz channels, 1/2 DPC	12 DDR5 max. 4800 MHz channels, 1/2 DPC	Six DDR5 max. 4800 MHz channels, 1/2 DPC
PCIe configuration	• PCIe 4.0, 128 lanes per socket • 128 to 160 lanes on a 2P node, 16 SATA lanes	• PCIe 5.0, 128 lanes per socket • 128 to 160 lanes on a 2P node Bonus 8 PCIe 3.0 lanes, 4 lanes per socket • 12 lanes in a 2P configuration, 32 SATA lanes per socket on P0/G3	• PCIe 5.0, 96 lane • Bonus 8 PCIe 3.0 lanes, 32 SATA lanes (shared with PCIe 5.0 on P0/G3)
CXL1.1+ configuration	N/A	64 lanes on P links configured for CXL1.1+	48 lanes on P links configured for

EPYC platform specification comparisons

Scroll down for more information

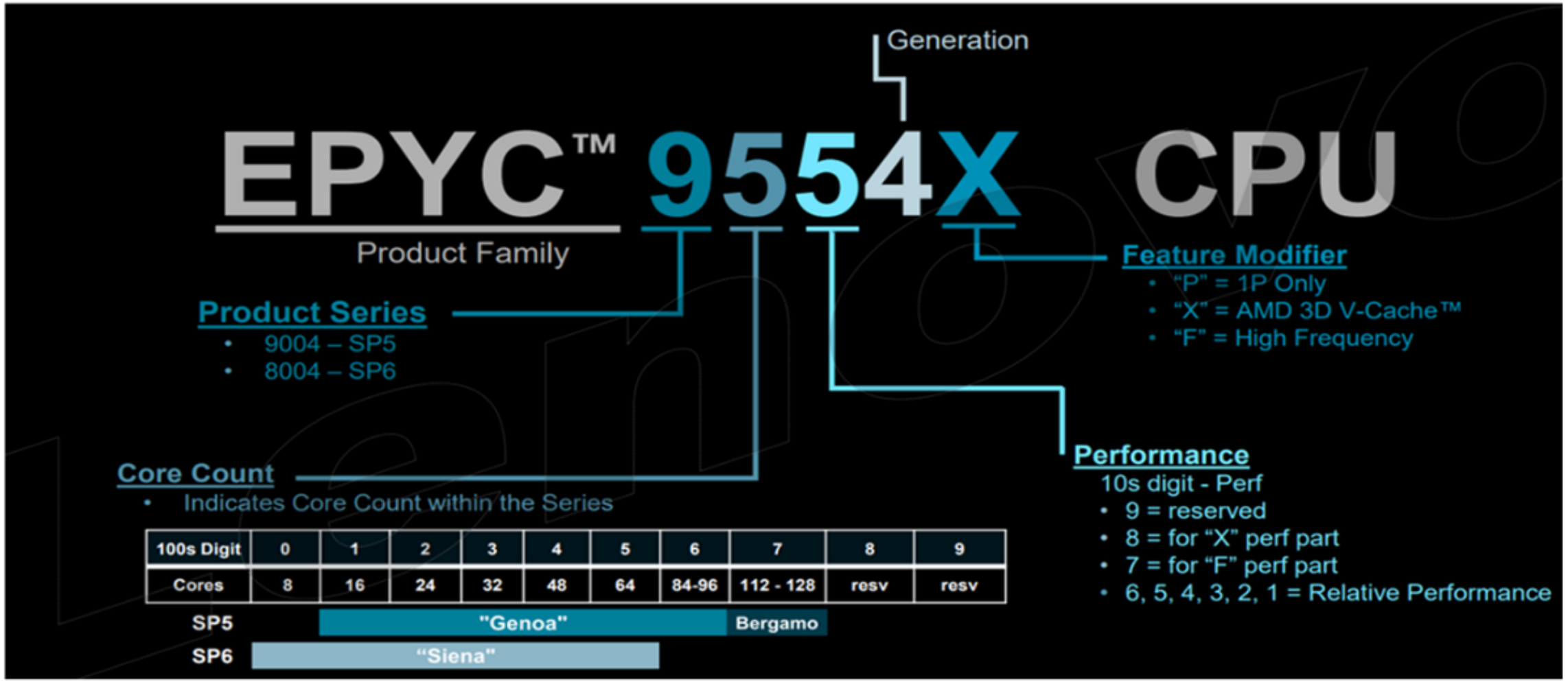
Platform	SP3	SP5	SP6
TDP	120 to 280 W	200 to 400 W	70 to 225 W
Memory configuration	Eight DDR4 3200 MHz channels, 1/2 DPC	12 DDR5 max. 4800 MHz channels, 1/2 DPC	Six DDR5 max. 4800 MHz channels, 1/2 DPC
PCIe configuration	• PCIe 4.0, 128 lanes per socket • 128 to 160 lanes on a 2P node, 16 SATA lanes	• PCIe 5.0, 128 lanes per socket • 128 to 160 lanes on a 2P node Bonus 8 PCIe 3.0 lanes, 4 lanes per socket • 12 lanes in a 2P configuration, 32 SATA lanes per socket on P0/G3	• PCIe 5.0, 96 lane • Bonus 8 PCIe 3.0 lanes, 32 SATA lanes (shared with PCIe 5.0 on P0/G3)
CXL1.1+ configuration	N/A	64 lanes on P links configured for CXL1.1+	48 lanes on P links configured for CXL1.1+
xGMI (Socket to Socket)	Three to four links, 2nd Gen Infinity 16 Gbps	Three to four links, 3rd Gen Infinity up to 32 Gbps	N/A – 1P only
I/O and xGMI configuration	Rear I/O, front XGMI	New topology support added – front and rear I/O	
DIMM types	RDIMM, LRDIMM, 3DS RDIMM	RDIMM, 3DS RDIMM	RDIMM, 3DS RDIMM

EPYC Zen4 processor



Lenovo

EPYC Zen4 processor naming convention



EYPC 9004 series CPUs (1)

CPU name	Architecture	Family	Total CCDs	Cores / threads	L3 cache	Base / max clocks	TDP / cTDP	CPU positioning
EPYC 9754	4 nm Zen 4C	Bergamo	8	128/256	256 MB	2.05-3.20 GHz	360 W (320-400 W)	Density optimized
EPYC 9734	4 nm Zen 4C	Bergamo	8	112/224	256 MB	2.00-3.20 GHz	340 W (320-400 W)	Density optimized
EPYC 9654P	5 nm Zen 4	Genoa	12	96/192	384 MB	2.05-3.70 GHz	360 W (320-400 W)	Density optimized
EPYC 9654	5 nm Zen 4	Genoa	12	96/192	384 MB	2.05-3.70 GHz	360 W (320-400 W)	Density optimized
EPYC 9634	5 nm Zen 4	Genoa	8	84/168	384 MB	2.00-3.70 GHz	290 W (240-300 W)	Density optimized
EPYC 9554P	5 nm Zen 4	Genoa	8	64/128	256 MB	2.70-3.70 GHz	360 W (320-400 W)	Density optimized
EPYC 9534	5 nm Zen 4	Genoa	8	64/128	256 MB	2.30-3.70 GHz	280 W (240-300 W)	Balanced

EYPC 9004 series CPUs (2)

CPU name	Architecture	Family	Total CCDs	Cores / threads	L3 cache	Base / max clocks	TDP / cTDP	CPU positioning
EPYC 9534	5 nm Zen 4	Genoa	8	64/128	256 MB	2.30-3.70 GHz	280 W (240-300 W)	Balanced
EPYC 9454P	5 nm Zen 4	Genoa	8	48/96	256 MB	2.25-3.70 GHz	290 W (240-300 W)	Balanced
EPYC 9454	5 nm Zen 4	Genoa	8	48/96	256 MB	2.25-3.70 GHz	290 W (240-300 W)	Balanced
EPYC 9354P	5 nm Zen 4	Genoa	8	32/64	256 MB	2.75-3.70 GHz	280 W (240-300 W)	Core strength
EPYC 9354	5 nm Zen 4	Genoa	8	32/64	256 MB	2.75-3.70 GHz	280 W (240-300 W)	Core strength
EPYC 9344	5 nm Zen 4	Genoa	4	32/64	128 MB	2.50-3.70 GHz	210 W (200-240 W)	Balanced
EPYC 9254	5 nm Zen 4	Genoa	4	24/48	128 MB	2.40-3.70 GHz	200 W (200-240 W)	Balanced

EYPC 9004 series CPUs (3)

CPU name	Architecture	Family	Total CCDs	Cores / threads	L3 cache	Base / max clocks	TDP / cTDP	CPU positioning
EPYC 9224	5 nm Zen 4	Genoa	4	24/48	64 MB	2.15-3.70 GHz	200 W (200-240 W)	Cost optimized
EPYC 9124	5 nm Zen 4	Genoa	4	16/32	64 MB	2.60-3.70 GHz	200 W (200-240 W)	Cost optimized
EPYC 9474F	5 nm Zen 4	Genoa	8	48/96	256 MB	3.20-4.00 GHz+	360 W (320-400 W)	Frequency optimized
EPYC 9374F	5 nm Zen 4	Genoa	8	32/64	256 MB	3.30-4.00 GHz+	320 W (320-400 W)	Frequency optimized
EPYC 9274F	5 nm Zen 4	Genoa	8	24/48	256 MB	3.30-4.00 GHz+	320 W (320-400 W)	Frequency optimized
EPYC 9174F	5 nm Zen 4	Genoa	8	16/32	256 MB	3.60-4.00 GHz+	320 W (320-400 W)	Frequency optimized