Smarter technology for all

AMD EPYC processor architecture for ThinkSystem V3 servers

ES42430

December 2022

Prerequisites

Although there are no specific prerequisites for this course, you should have some knowledge of high performance computing (HPC) systems, be familiar with the general administration of a network cluster, and have problem determination and troubleshooting skills.

Objectives

After completing the course, you will be able to:

- Describe the key components and technology of the EPYC platforms
- Describe the ThinkSystem support for AMD processor levels and features
- Describe memory support and configuration rules
- Describe AMD processor heat sink and hardware features

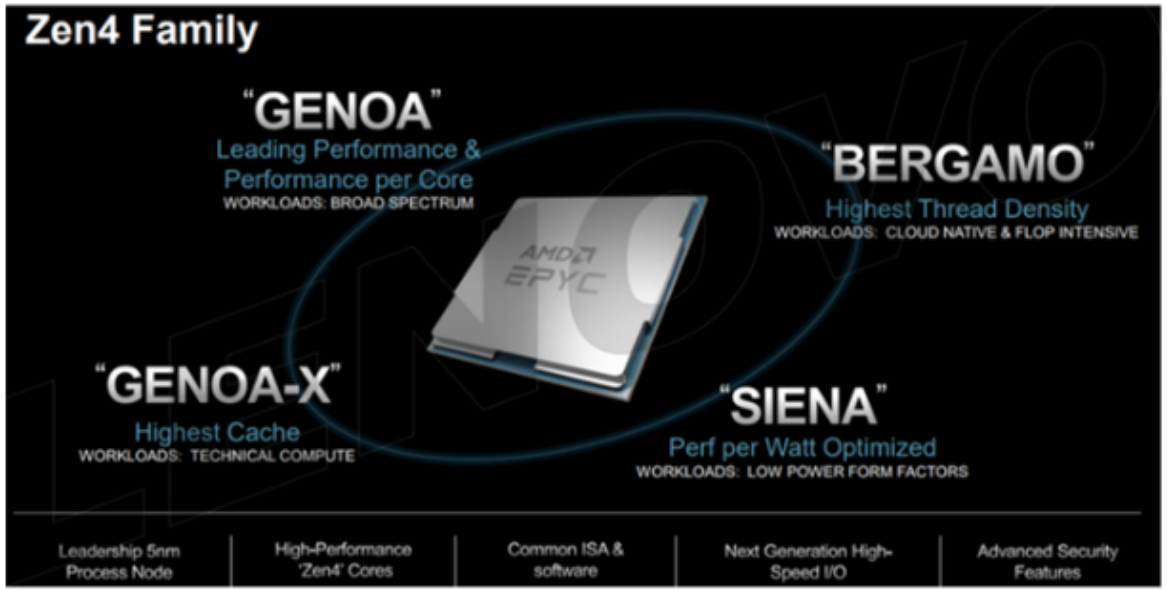
EPYC processor overview

EPYC platform design

Fourth generation EPYC processor overview

EPYC is a brand of x86-64 processors designed and marketed by AMD. They are based on the company's Zen microarchitecture and are specifically targeted for the server and embedded system market. The “Genoa” processor is part of the fourth generation of the EPYC processor family.

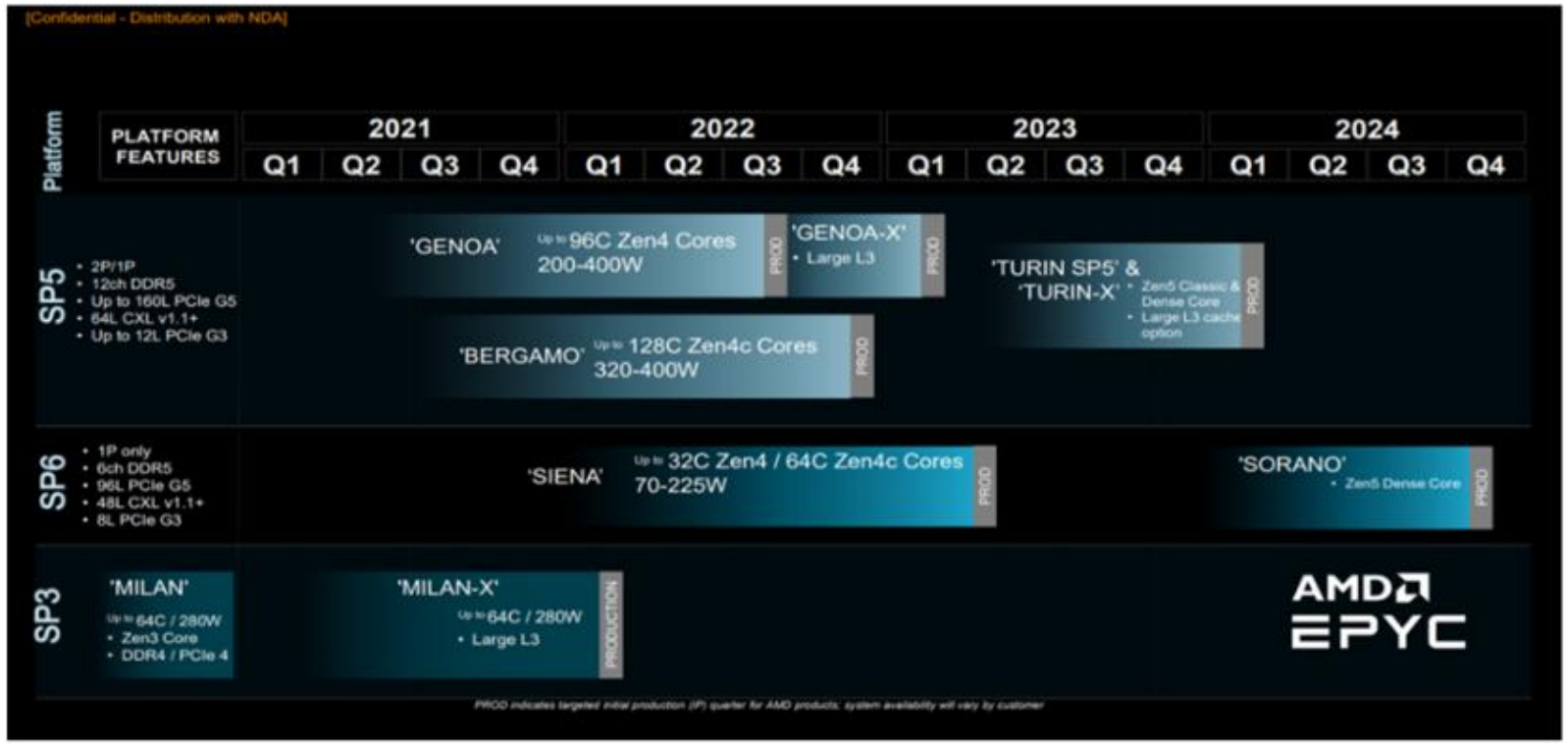
Genoa processors, branded the EPYC 9004 series, are available in a 6096-contact land grid array package for Socket SP5. They have a TDP of up to 320 W and a configurable TDP reaching 400 W. They support 12 channels of DDR5-4800 memory and 128 PCIe 5.0 lanes per socket, and up to 160 lanes in total on two-processor systems (the same as previous generations). Genoa processors implement up to 96 cores with two-way SMT and 192 threads per socket.



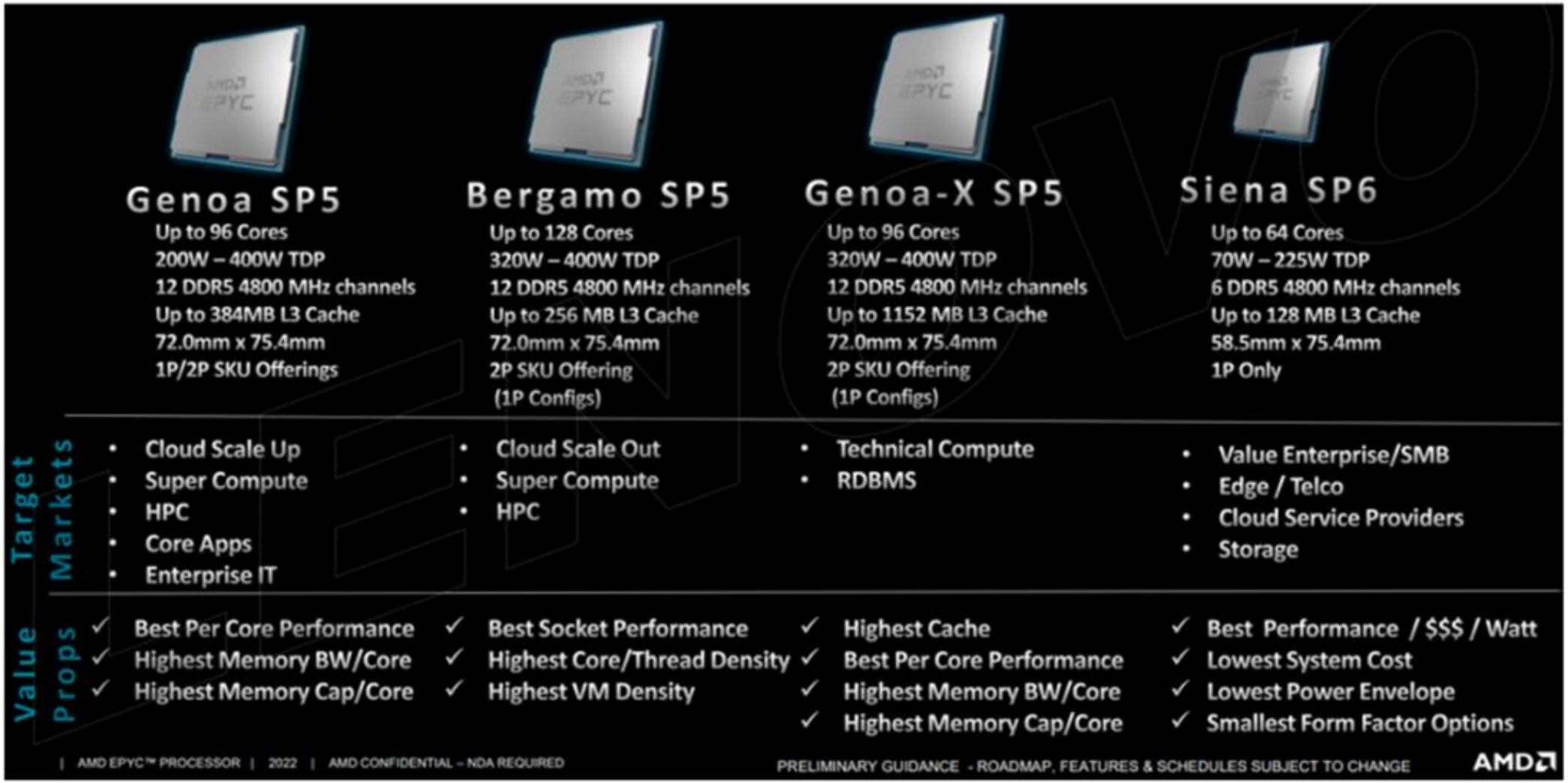
EPYC platform roadmap

The AMD Zen 4 with SP5 socket lineup will be split into three families: the standard Zen 4 EPYC Genoa series, the compute density-optimized Zen 4C EPYC Bergamo series, and the cache-optimized Zen 4 V-Cache EPYC Genoa-X series.

There will also be an entry-level server offering called the EPYC Siena, branded the EPYC 8004, which will use the same Zen 4 cores but with the TCO-optimized SP6 socket.



Zen4 family comparison

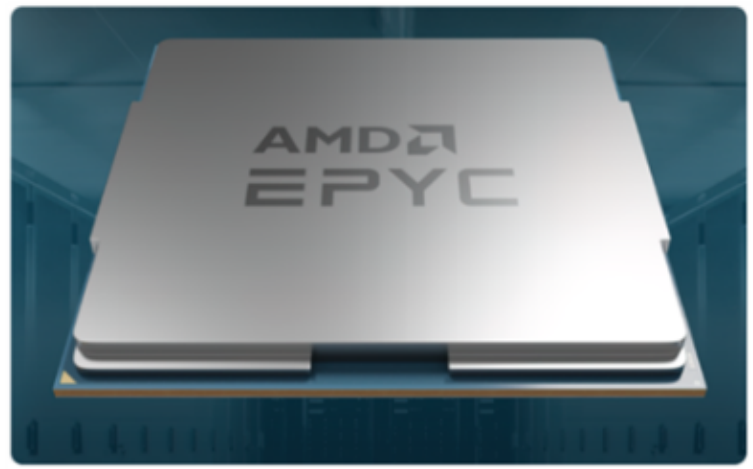


EPYC Genoa processor overview (1)

The EPYC Genoa processor supports up to 96 cores with the new SP5 socket – each socket supports up to 12 CCDs (Core Chiplet Die). The processors support PCIe 5.0, DDR5, and a TDP of up to 400 W.

Compute

- AMD Zen4 x86 cores (Up to 12 CCDs, 96 cores, and 192 threads)
- 1 MB of L2 cache per core (Up to 32 MB of L3 cache per CCD)
- Updated IOD and internal AMD Gen3 Infinity Fabric™
- Architecture with increased die-to-die bandwidth



Memory support

- 12 channel DDR5 with ECC up to 4800 MHz
- Optional 2, 4, 6, 8, 10, or 12 channel memory interleaving
- Support for RDIMMs and 3DS RDIMMs
- Up to two DIMMs per channel and a capacity of 6 TB per socket (256 GB 3DS RDIMMs)

EPYC Genoa processor overview (2)

Integrated I/O

- Up to 160 I/O lanes (with two processors) of PCIe 5.0 with speeds of up to 32 Gbps and bifurcations supported down to x1
- Bonus PCIe 3.0 lanes
  - Up to 12 lanes in a two-processor configuration
  - Up to eight lanes in a one-processor configuration
- Support for SDCI (Smart Data Cache Injection)
- 64 I/O lanes with support for CXL1.1+ and bifurcations supported down to x4

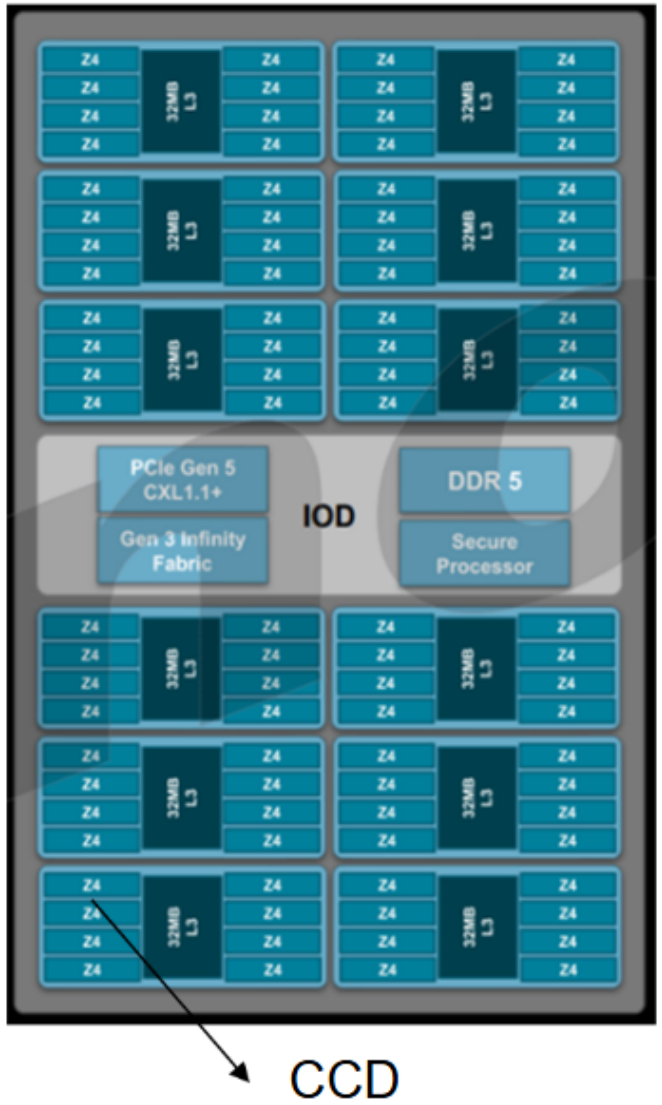
SP5 platform

- New socket with increased power delivery and VR (voltage regulator)
- Up to four Gen3 AMD Infinity Fabric™ links with speeds of up to 32 Gbps

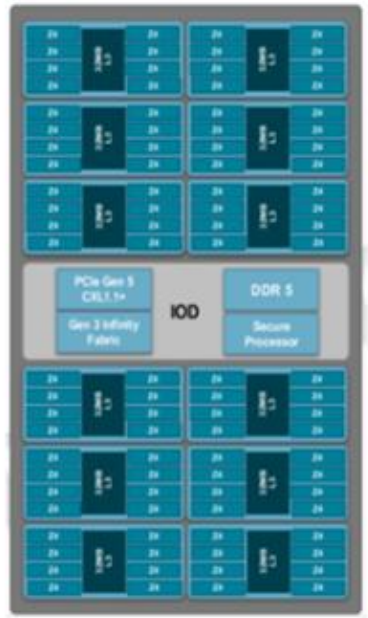
Security

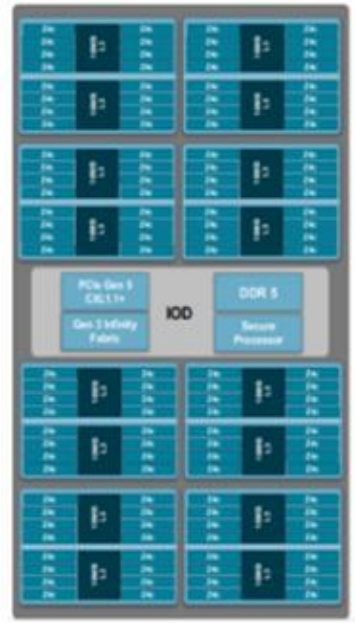
- Decicated security subsystem with enhancements
- Hardware Root of Trust

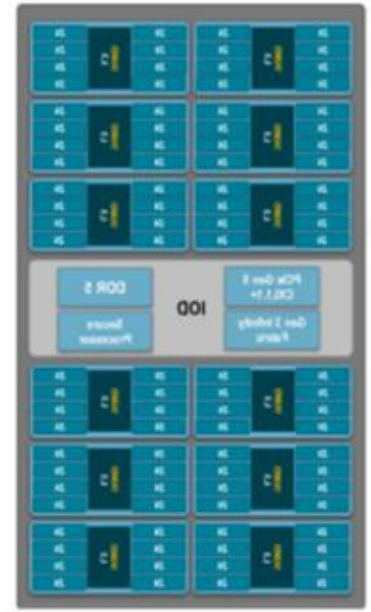
Note: For more information about EPYC features, refer to the AMD website



EPYC SP5 platform processor comparison







EPYC	Genoa SP5	Bergamo SP5	Genoa-X SP5
Zen	Zen4 performance optimized	Zen4 power optimized	Zen4 performance optimized
CCD	Up to 96 cores, 192 threads, 8 cores per CCD, and 12 CCDs	Up to 128 cores, 256 threads, 8 cores per CCD, and 8 CCDs	Up to 96 cores, 192 threads, 8 cores per CCD, and 12 CCDs
L3 Cache	Up to 384 MB 32 MB per CCD	Up to 256 MB 32 MB per CCD	Up to 1152 MB 96 MB per CCD
Common specifications	A TDP of up to 400 W, 12 channels of DDR5-4800, up to 32 GT xGMI, 128 lanes of HSIO (32 GT/s), AGESA GenoaPI-SP5		