Smarter technology for all

ThinkSystem server architecture – AMD EPYC processor models

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Lenovo

Prerequisites

Although there are no specific prerequisites for this course, you should have some knowledge of high performance computing (HPC) systems, be familiar with the general administration of ThinkSystem servers, and have problem determination and troubleshooting skills.

Objectives

After completing the course, you will be able to:

- Describe the key components and technology of the AMD EPYC platforms
- Describe Lenovo ThinkSystem support for AMD processor levels and features
- Describe memory support and configuration rules
- Describe AMD processor heat sink and hardware features

AMD EPYC processor overview

Common AMD EPYC platform design

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AMD EPYC 2nd generation processor overview

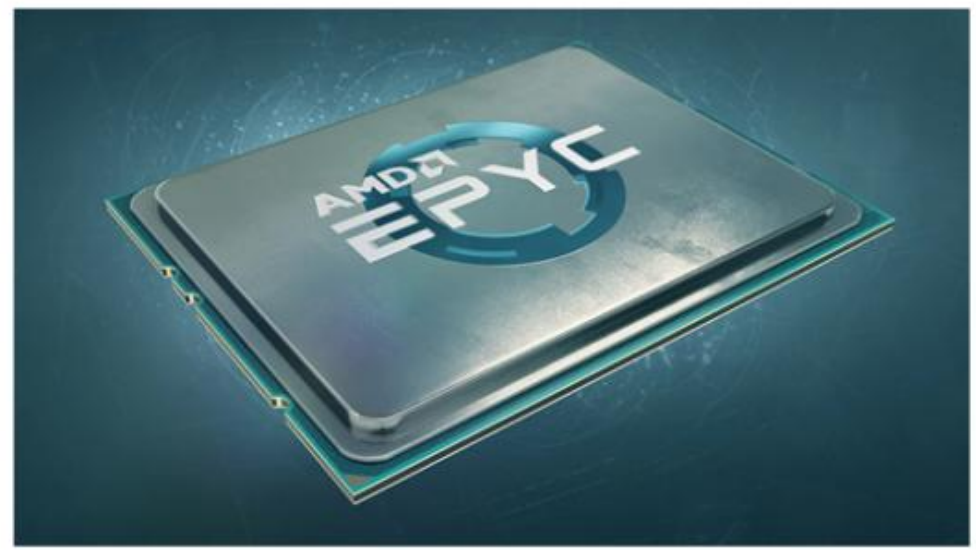
AMD EPYC is a brand of x86-64 processors designed and marketed by **AMD**. They are based on the company's Zen microarchitecture and are specifically targeted for the server and embedded system market. The Rome processor is the 2nd generation of the AMD EPYC processor family.

Compute node

- Up to 64 AMD “Zen2” x86 cores (128 threads)
- 512 KB L2 cache per core (32 MB total L2 cache)
  - 16 MB shared L3 per 4 cores (256 MB total L3 cache)
  - Platform Security Processor

Memory support

- 8 channel DDR4 with ECC up to 3200 MHz
- RDIMM, LRDIMM, NVDIMM-N, 3DS DIMM
- 2 DIMMs per channel
- Memory capacity:
  - 2 TB per socket with 8 Gb devices
  - 4 TB per socket with 16 Gb devices
  - S-Link (CCIX 2.0) support on two 16 bit “P” links



AMD EPYC processor overview

Integrated I/O

- One processor:
  - 128 lanes PCIe Gen4 + 2 lanes Gen2 (BMC, etc)
  - 32 lanes switchable to SATA
- Server Controller Hub (USB, UART, SPI, LPC, I2C, etc.)

Note: For more information about AMD EPYC features, please refer to the AMD EPYC Web site.