System configurations and diagrams
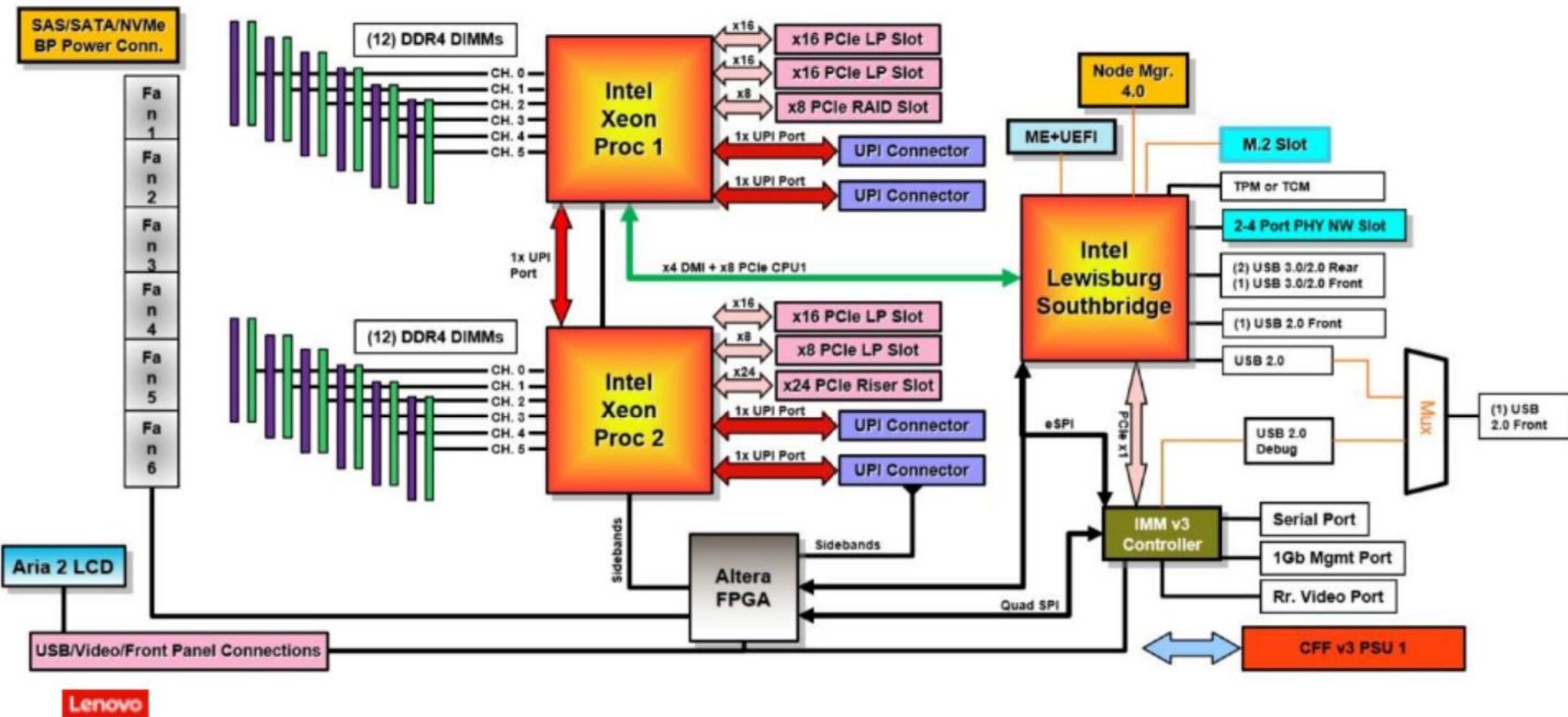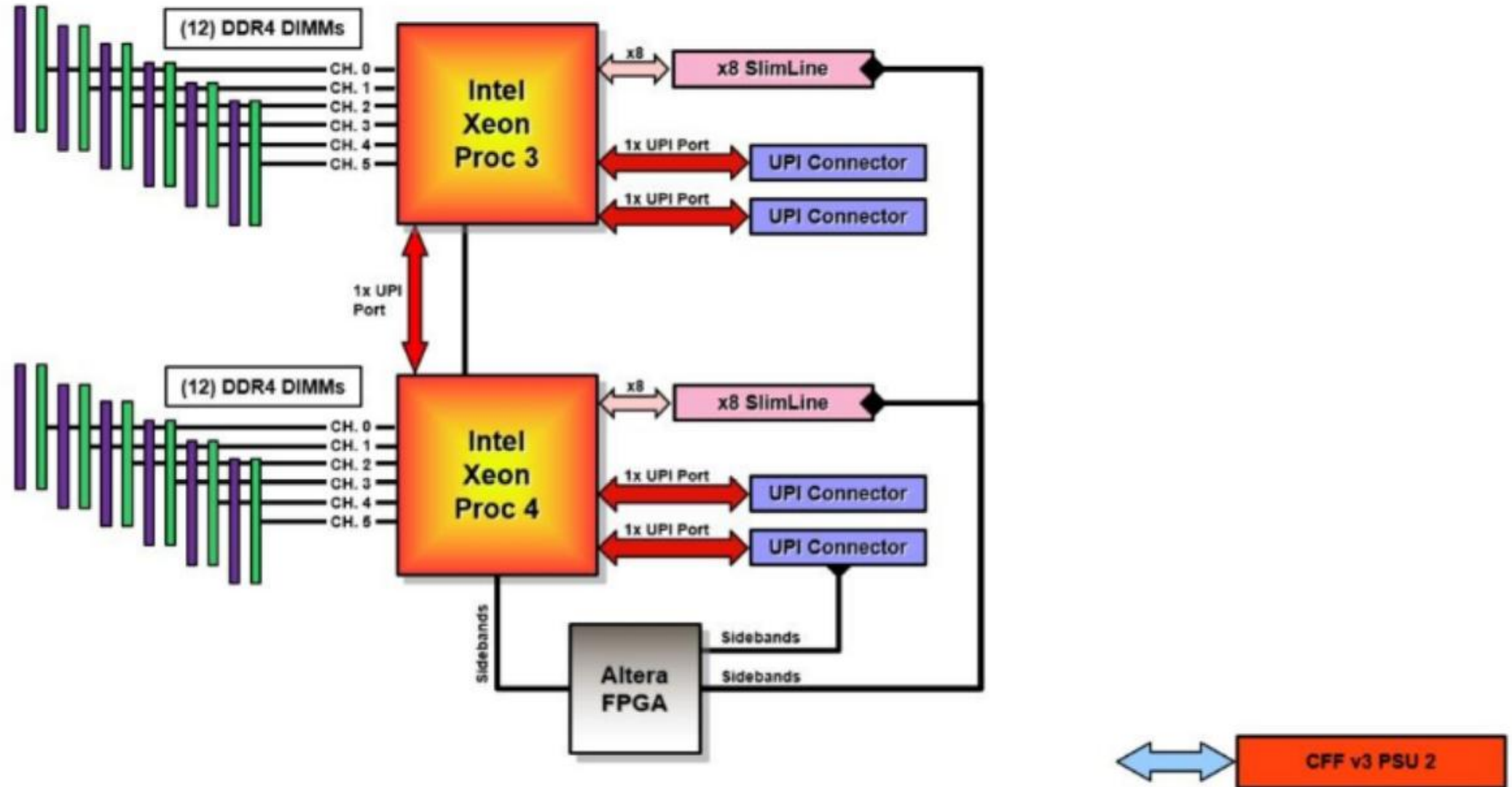
CPU, memory, PCIe riser, and storage configurations

SR850P system board block diagram

SAS/SATA/NVMe BP Power Conn.

(12) DDR4 DIMMs

Intel Xeon Proc 1
- CH. 0
- CH. 1
- CH. 2
- CH. 3
- CH. 4
- CH. 5

x16 — x16 PCIe LP Slot
x16 — x16 PCIe LP Slot
x8 — x8 PCIe RAID Slot
1x UPI Port — UPI Connector
1x UPI Port — UPI Connector

1x UPI Port

x4 DMI + x8 PCIe CPU1

Node Mgr. 4.0

ME+UEFI

Intel Lewisburg Southbridge

M.2 Slot
TPM or TCM
2-4 Port PHY NW Slot
(2) USB 3.0/2.0 Rear
(1) USB 3.0/2.0 Front
(1) USB 2.0 Front
USB 2.0

(12) DDR4 DIMMs

Intel Xeon Proc 2
- CH. 0
- CH. 1
- CH. 2
- CH. 3
- CH. 4
- CH. 5

x16 — x16 PCIe LP Slot
x8 — x8 PCIe LP Slot
x24 — x24 PCIe Riser Slot
1x UPI Port — UPI Connector
1x UPI Port — UPI Connector

Fan 1
Fan 2
Fan 3
Fan 4
Fan 5
Fan 6

Aria 2 LCD

Sidebands

Altera FPGA

Sidebands

eSPI

PCIe x1

USB 2.0 Debug

Mux

(1) USB 2.0 Front

IMM v3 Controller
- Serial Port
- 1Gb Mgmt Port
- Rr. Video Port

Quad SPI

USB/Video/Front Panel Connections

CFF v3 PSU 1

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SR850P processor and memory expansion board block diagram

Memory architecture

The SR850P supports many types of DDR4 DIMMs, including RDIMMs, LRDIMMs, 3DS RDIMMs, and Intel DC persistent memory modules (DCPMMs). Each processor contains two integrated memory controllers (IMCs), and each controller provides three DDR4 channels with two DIMMs per channel. There should be at least one DDR4 DIMM per processor.
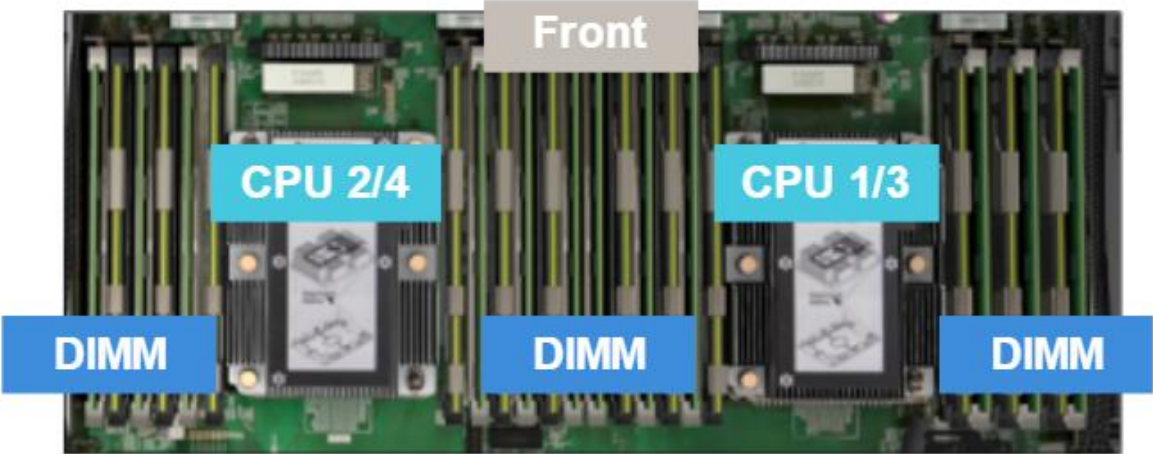
The SR850P supports the following memory modes:
- Independent memory mode
- Memory mirroring mode
- Memory sparing mode

The following memory modes are supported with DCPMMs:
- App Direct mode
- Memory mode
- Mixed Memory mode

DIMM slot numbering

The following table indicates the organization of channels and DIMM slots around a processor.

Slot	0	1	0	1	0	1	Processor	1	0	1	0	1	0
Channel	Channel 2		Channel 1		Channel 0			Channel 0		Channel 1		Channel 2	
DIMM number (Processor 1)	1	2	3	4	5	6		7	8	9	10	11	12
DIMM number (Processor 2)	13	14	15	16	17	18		19	20	21	22	23	24
DIMM number (Processor 3)	25	26	27	28	29	30		31	32	33	34	35	36
DIMM number (Processor 4)	37	38	39	40	41	42		43	44	45	46	47	48

Memory population rules

General population rules for DIMMs are as follows:
- Mixing RDIMMs and LRDIMMs is not supported.
- Mixing x4 and x8 DIMMs in the same channel is supported.
- Mixing memory vendors is supported, but only with Lenovo-qualified vendors.
- Mixing memory capacities is supported, but users must install higher capacity DIMMs first.
- Mixing memory ranks is supported. Always populate DIMMs with the largest number of ranks in slot 0 and then slot 1.
- If DIMMs with different frequencies are mixed in the same channel, all DIMMs will run at the lowest frequency.

Additional rules for system-level RAS Mode combination limitations:
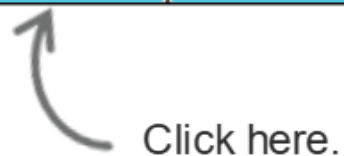- Mixing non-mirrored and mirrored mode is not allowed on the platform.
- Mixing sparing and mirrored mode is not allowed on the platform.
- Best RAS capability (and performance) requires two ranks per channel.
- Always populate DIMMs with the maximum number of ranks in the farthest DIMM slot, followed by the nearest DIMM slot.

Independent channel mode

All six channels can be populated in any order, and there are no DIMM-matching requirements in independent channel mode. However, all channels must run at the same interface frequency. Individual channels may run at different DIMM timings (RAS latency, CAS latency, and so on).

Click the highlighted areas to see the memory installation order in independent channel mode.

Installed DIMMs	Processor	
4 – 24 memory DIMMs	Processor 1 & 2	Processor 3 & 4
25 – 48 memory DIMMs	Processor 1 & 2	Processor 3 & 4

Click here.

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...in independent channel m... frequency. Individual char... and so on).

Click the highlighted area...

Installed DIM...

4 – 24 memory D...

25 – 48 memory D...

Total DIMMs	Processor 1												Processor 2												Total DIMMs
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
4								8												20					4
5					5			8												20					5
6					5			8									17			20					6
7					5			8									17			20					7
8					5			8									17			20					8
9					5			8		10							17			20					9
10					5			8		10							17			20		22			10
11					5			8		10							17			20		22			11
12					5			8		10							17			20		22			12
13			3		5			8		10							17			20		22			13
14			3		5			8		10					15		17			20		22			14
15			3		5			8		10					15		17			20		22			15
16			3		5			8		10					15		17			20		22			16
17			3		5			8		10		12			15		17			20		22			17
18			3		5			8		10		12			15		17			20		22		24	18
19			3		5			8		10		12			15		17			20		22		24	19
20			3		5			8		10		12			15		17			20		22		24	20
21	1		3		5			8		10		12			15		17			20		22		24	21
22	1		3		5			8		10		12	13		15		17			20		22		24	22
23	1		3		5			8		10		12	13		15		17			20		22		24	23
24	1		3		5			8		10		12	13		15		17			20		22		24	24

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Processors 1 and 2, with 25 to 48 DIMMs installed in the server

in independent channel mo...
frequency. Individual chann...
and so on).

Click the highlighted areas ...

Installed DIMMs

4 – 24 memory DIM...

25 – 48 memory DIM...

Total DIMMs	Processor 1												Processor 2												Total DIMMs
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
25	1		3		5		7	8	9	10			13		15		17			20		22		24	25
26	1		3		5		7	8	9	10			13		15		17		19	20	21	22			26
27	1		3		5		7	8	9	10			13		15		17		19	20	21	22			27
28	1		3		5		7	8	9	10			13		15		17		19	20	21	22			28
29			3	4	5	6	7	8	9	10			13		15		17		19	20	21	22			29
30			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			30
31			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			31
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			32
33	1		3		5		7	8	9	10	11	12			15	16	17	18	19	20	21	22			33
34	1		3		5		7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	34
35	1		3		5		7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	35
36	1		3		5		7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	36
37			3	4	5	6	7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	37
38			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	38
39			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	39
40			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	40
41	1	2	3	4	5	6	7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	41
42	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	42
43	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	43
44	1		3	4	5	6	7	8	9	10	11	12	13		15	16	17	18	19	20	21	22	23	24	44
45	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	45
46	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	46
47	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	47
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	48

in independent channel m...
frequency. Individual char...
and so on).

Click the highlighted area...

Installed DIMM...

4 – 24 memory DI...

25 – 48 memory D...

Total DIMMs	Processor 3												Processor 4												Total DIMMs
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	
4								32												44					4
5								32												44					5
6								32												44					6
7					29			32												44					7
8					29			32									41			44					8
9					29			32									41			44					9
10					29			32									41			44					10
11					29			32		34							41			44					11
12					29			32		34							41			44		46			12
13					29			32		34							41			44		46			13
14					29			32		34							41			44		46			14
15			27		29			32		34							41			44		46			15
16			27		29			32		34					39		41			44		46			16
17			27		29			32		34					39		41			44		46			17
18			27		29			32		34					39		41			44		46			18
19			27		29			32		34		36			39		41			44		46			19
20			27		29			32		34		36			39		41			44		46		48	20
21			27		29			32		34		36			39		41			44		46		48	21
22			27		29			32		34		36			39		41			44		46		48	22
23	25		27		29			32		34		36			39		41			44		46		48	23
24	25		27		29			32		34		36	37		39		41			44		46		48	24

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...nts in independent channel mo... frequency. Individual chan..., and so on).

Click the highlighted areas ...le.

Installed DIMM

4 – 24 memory DIM...

25 – 48 memory DI...

Total DIMMs	Processor 3												Processor 4												Total DIMMs
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	
25	25		27		29			32		34		36	37		39		41			44		46		48	25
26	25		27		29			32		34		36	37		39		41			44		46		48	26
27	25		27		29		31	32	33	34			37		39		41			44		46		48	27
28	25		27		29		31	32	33	34			37		39		41		43	44	45	46			28
29	25		27		29		31	32	33	34			37		39		41		43	44	45	46			29
30	25		27		29		31	32	33	34			37		39		41		43	44	45	46			30
31			27	28	29	30	31	32	33	34			37		39		41		43	44	45	46			31
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			32
33			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			33
34			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			34
35	25		27		29		31	32	33	34	35	36			39	40	41	42	43	44	45	46			35
36	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	36
37	25		27		29		31	32	33	34	35	36	37	38	39		41		43	44	45	46	47	48	37
38	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	38
39			27	28	29	30	31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	39
40			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	40
41			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	41
42	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	42
43			27	28	29	30	31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	43
44	25		27	28	29	30	31	32	33	34	35	36	37		39	40	41	42	43	44	45	46	47	48	44
45	25	26	27	28	29	30	31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	45
46	25	26	27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	46
47	25	26	27	28	29	30	31	32	33	34	35	36	37		39	40	41	42	43	44	45	46	47	48	47
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	48

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Memory mirroring mode

Memory mirroring mode gives users full memory redundancy but cuts the total system memory capacity in half. Memory channels are grouped in pairs with both channels in a pair receiving the same data. If a failure occurs, the memory controller switches from the DIMMs on the primary channel to the DIMMs on the backup channel.

• Each DIMM must be identical in size and architecture.
• DIMMs on each memory channel must be of equal density.
• If two memory channels have DIMMs, mirroring occurs across two DIMMs (channels 0/1 will both contain the primary/secondary memory caches).
• If three memory channels have DIMMs, mirroring occurs across all three DIMMs (channels 0/1, channels 1/2, and channels 2/0 will all contain primary/secondary memory caches).

Click the highlighted areas to see the memory installation order in memory mirroring mode.

Installed DIMMs	Processor	
Eight to 48 DIMMs	Processors 1 & 2	Processors 3 & 4

Click here.

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memory capacity in half.
receiving the same data.
on the primary channel to
• Each DIMM must be id
• DIMMs on each memor
• If two memory channels
  both contain the primar
• If three memory channe
  0/1, channels 1/2, and

Click the highlighted area

Installed DIMMs

Eight to 48 DIMMs

Total DIMMs	Processor 1												Processor 2												Total DIMMs
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
8								8		10										20		22			8
10								8		10		12								20		22			10
12			3		5			8		10										20		22			12
14			3		5			8		10										20		22		24	14
16			3		5			8		10					15		17			20		22			16
18	1		3		5			8		10		12			15		17			20		22			18
20	1		3		5			8		10		12			15		17			20		22			20
22	1		3		5			8		10		12	13		15		17			20		22		24	22
24	1		3		5			8		10		12	13		15		17			20		22		24	24
26			3	4	5	6	7	8	9	10			13		15		17			20		22		24	26
28			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			28
30			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			30
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			32
34	1	2	3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22			34
36	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	36
38	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	38
40	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	40
42	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	42
44	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	44
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	48

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Click here.

memory capacity in half.
receiving the same data.
on the primary channel to
• Each DIMM must be ide
• DIMMs on each memor
• If two memory channels
  both contain the primar
• If three memory channe
  0/1, channels 1/2, and

Click the highlighted area

Installed DIMMs

Eight to 48 DIMMs

Total DIMMs	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	Total DIMMs
8								32		34										44		46			8
10								32		34		36								44		46			10
12			27		29			32		34										44		46			12
14			27		29			32		34										44		46		48	14
16			27		29			32		34					39		41			44		46			16
18			27		29			32		34					39		41			44		46			18
20	25		27		29			32		34		36			39		41			44		46			20
22	25		27		29			32		34		36			39		41			44		46			22
24	25		27		29			32		34		36	37		39		41			44		46		48	24
26	25		27		29			32		34		36	37		39		41			44		46		48	26
28	25		27		29			32		34		36	37		39		41			44		46		48	28
30			27	28	29	30	31	32	33	34			37		39		41			44		46		48	30
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			32
34			27	28	29	30	31	32	33	34			37		39		41			44		46		48	34
36	25		27		29			32		34		36	37		39		41			44		46		48	36
38			27	28	29	30	31	32	33	34			37		39		41			44		46		48	38
40			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			40
42	25	26	27	28	29	30	31	32	33	34	35	36	37		39		41			44		46		48	42
44	25	26	27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46			44
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	10	41	42	43	44	45	46	47	48	48

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Click here.

Rank sparing mode

In rank sparing mode, one or more ranks are spares for the other ranks on the same channel. The spare rank(s) are held in reserve and are not available as system memory. The spare rank(s) must have a memory capacity that is identical to or larger than that of any of the other ranks (sparing source ranks) on the same channel. After sparing, the sparing source rank will no longer be available as system memory.

- When adding one or more DIMMs during a memory upgrade, the user might need to move some pre-installed DIMMs to new locations.
- An even number of DIMMs is required for memory sparing.

Click the highlighted areas to see the memory installation order in rank sparing mode.

Installed DIMMs	Processor	
Eight to 48 DIMMs	Processors 1 & 2	Processors 3 & 4

Click here.

The spare rank(s) are hel...
rank(s) must have a mem...
ranks (sparing source ran...
no longer be available as...
• When adding one or m...
   some pre-installed DIM...
• An even number of DIM...

Click the highlighted area...

Installed DIMMs

Eight to 48 DIMMs

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Total DIMMs	Processor 1												Processor 2												Total DIMMs
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
8							7	8											19	20					8
10					5	6	7	8											19	20					10
12					5	6	7	8									17	18	19	20					12
14					5	6	7	8									17	18	19	20					14
16					5	6	7	8									17	18	19	20					16
18					5	6	7	8	9	10							17	18	19	20					18
20					5	6	7	8	9	10							17	18	19	20	21	22			20
22					5	6	7	8	9	10							17	18	19	20	21	22			22
24					5	6	7	8	9	10							17	18	19	20	21	22			24
26			3	4	5	6	7	8	9	10							17	18	19	20	21	22			26
28			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			28
30			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			30
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			32
34			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22			34
36			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	36
38			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	38
40			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	40
42	1	2	3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	42
44	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	44
46	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	46
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	48

Processors 3 and 4, with eight to 48 DIMMs installed in the server

The spare rank(s) are he
rank(s) must have a mem
ranks (sparing source rar
no longer be available as
• When adding one or mc
   some pre-installed DIM
• An even number of DIM

Click the highlighted area

Installed DIMMs

Eight to 48 DIMMs

Total DIMMs	Processor 3												Processor 4												Total DIMMs
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	
8							31	32											43	44					8
10							31	32											43	44					10
12							31	32											43	44					12
14					29	30	31	32											43	44					14
16					29	30	31	32									41	42	43	44					16
18					29	30	31	32									41	42	43	44					18
20					29	30	31	32									41	42	43	44					20
22					29	30	31	32	33	34							41	42	43	44					22
24					29	30	31	32	33	34							41	42	43	44	45	46			24
26					29	30	31	32	33	34							41	42	43	44	45	46			26
28					29	30	31	32	33	34							41	42	43	44	45	46			28
30			27	28	29	30	31	32	33	34							41	42	43	44	45	46			30
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			32
34			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			34
36			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			36
38			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46			38
40			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	40
42			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	42
44			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	44
46	25	26	27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	46
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	48

DCPMM and DRAM DIMM installation order

Before installing DCPMMs and DRAM DIMMs, refer to the "DC Persistent Memory Module (DCPMM) setup" section in the *Setup Guide* and make sure all the requirements are met.

- To verify whether the installed processors support DCPMMs, check the four digits in the processor description. Only processor descriptions that meet both of the following requirements support DCPMMs.
- The first digit is a **5** or a larger number. The only exception to this rule is the *Intel Xeon Silver 4215*, which also supports DCPMMs.
- The second digit is a **2** – for example, the *Intel Xeon 52*15L and *Xeon Platinum 82*80M.
- If the installed processors do not support DCPMMs, replace the processors before installing DCPMMs.

Supported memory capacity range varies with the following types of DCPMMs.

- **Large memory tier (L):** Processors with an **L** after the four digits – for example, the *Intel Xeon 52*15L.
- **Medium memory tier (M):** The processors with an **M** after the four digits – for example, the *Xeon Platinum 82*80M.
- **Other:** Other processors that support DCPMMs – for example, the *Intel Xeon Gold 5222*.

Note: You can also check [memory configurator](#) for details.

Non-interleaved and interleaved DCPMM configurations

The App Direct mode configuration options using four DCPMMs per CPU socket are shown below. The figure on the left shows a non-interleaved module configuration, meaning each module is its own separate space. After namespaces are created, the operating system will see four devices. The figure on the right shows a single interleaved device using all four modules. The operating system will recognize this as one large device after a namespace is created.

Users can configure the regions either n-way (non-interleaved with one region per memory module) or 1-way (interleaved with one region that spans all modules). There is no option to select the interleaving width, meaning you cannot interleave a subset of available DCPMMs.

Non-Interleaved Regions

DIMM0   DIMM1   DIMM2   DIMM3

Interleaved Regions

DIMM0   DIMM1   DIMM2   DIMM3

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App Direct mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

Click the configurations for details.

Interleaved

Non-interleaved

- D: DRAM DIMMs with 16 GB or larger capacity
- P: DC Persistent Memory Module (DCPMM)

Configuration	Processor 1 / Processor 3												Processor 2 / Processor 4											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	P		D		D			D		D		P	P		D		D			D		D		P
8 DCPMMs and 32 DIMMs	P		D	D	D	D	D	D	D	D		P	P		D	D	D	D	D	D	D	D		P
8 DCPMMs and 24 DIMMs	D		D		D	P	P	D		D		D	D		D		D	P	P	D		D		D
16 DCPMMs and 24 DIMMs	D		D	P	D	P	P	D	P	D		D	D		D	P	D	P	P	D	P	D		D
24 DCPMMs and 24 DIMMs	D	P	D	P	D	P	P	D	P	D	P	D	D	P	D	P	D	P	P	D	P	D	P	D

Lenovo

App Direct mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

Click the configurations for details.

Interleaved

Non-interleaved

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1 DCPMM and 24 DIMMs	D		D		D		P	D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		P	D		D		D	D		D		D		P	D		D		D

Configuration	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
1 DCPMM and 24 DIMMs	D		D		D			D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		P	D		D		D	D		D		D		P	D		D		D

App Direct mode supported DCPMM capacity

Click the configurations to see the supported DCPMM capacities.

Interleaved

Non-interleaved

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	X
8	32	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		
24	24	L	√	√	√
		M	√	√	
		Other	√		

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App Direct mode supported DCPMM capacity

Click the configurations to see the supported DCPMM capacities.

Interleaved

Non-interleaved

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	24	L	√	√	√
		M	√	√	√
		Other	√	√	√
4	24	L	√	√	√
		M	√	√	√
		Other	√	√	

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Internal storage

The SR850P supports various internal storage configurations based on two different backplanes, for a total of up to 16 drives.

- 2.5-inch SAS/SATA eight-bay backplane
- 2.5-inch AnyBay eight-bay backplane
  - Eight 2.5-inch SAS or SATA drives
  - Four 2.5-inch SAS or SATA drives + four 2.5-inch U.2 (NVMe) drives

An AnyBay backplane supports four SAS/SATA bays and four AnyBay bays. The four AnyBay bays support SAS/SATA/NVMe as long as the RAID/HBA/NVMe controller is properly connected to the AnyBay backplane.

2.5-inch AnyBay eight-bay backplane

2.5-inch SATA/SAS eight-bay backplane

↑ Front
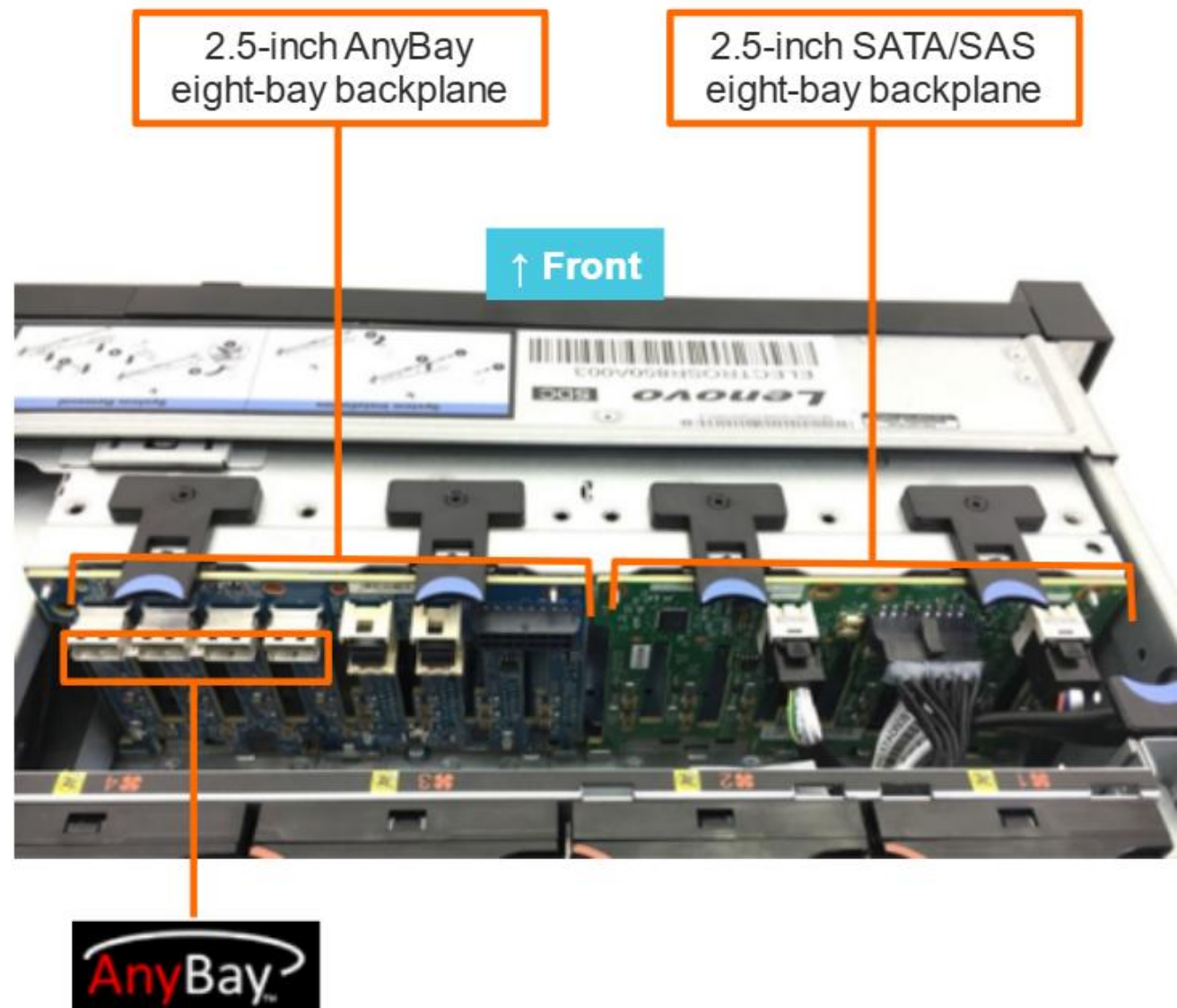
AnyBay

SR850P HDD drive configurations

The SR850P has five storage backplane combinations:

- Eight drive bays, all SAS/SATA
- Eight drive bays, where four are AnyBay bays
- Sixteen drive bays, all SAS/SATA
- Sixteen drive bays, where four are AnyBay bays
- Sixteen drive bays, where eight are AnyBay bays

Eight SATA/SAS

Four SATA/SAS + four AnyBay bays

16 SATA/SAS

12 SATA/SAS + four AnyBay bays

Eight SATA/SAS + eight AnyBay bays

Eight drive bays, all SAS/SATA

At least one eight-port SAS/SATA RAID adapter (530-8i or 930-8i) or HBA card (430-8i) is required to support this backplane. All eight drives will be connected to the adapter using two backplane cables.

Eight-port adapter
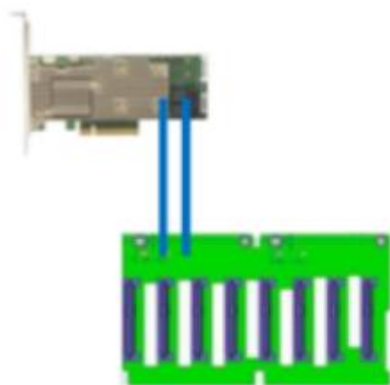
Eight drive bays, where four are AnyBay bays

At least one eight-port SAS/SATA RAID adapter or HBA card is required to support this backplane. The NVMe ports on the processor and memory expansion tray are used to connect to the NVMe connectors on the backplane.

Eight-port adapter
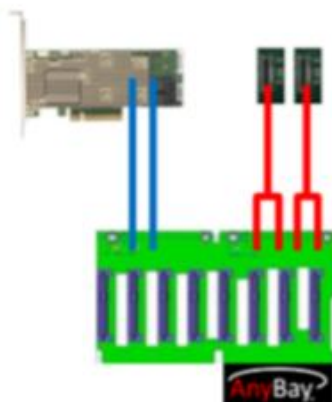
Onboard NVMe ports

Sixteen drive bays, all SAS/SATA

In this configuration, users can use either one 16i (930-16i or 430-16i) or two 8i adapters to support these backplanes.

A.

One 16-port adapter
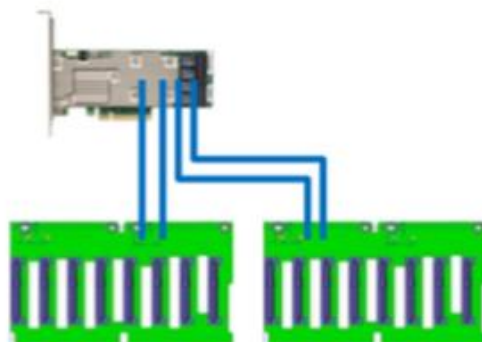
B.

Two eight-port adapters
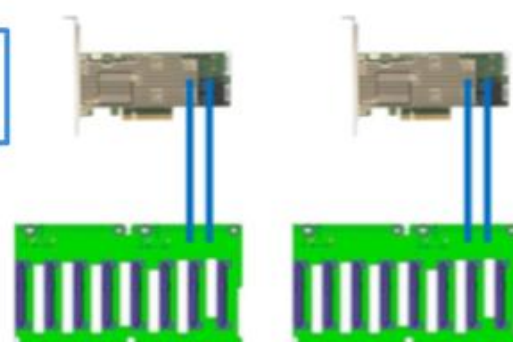
Sixteen drive bays, where four are AnyBay bays – four processors

In this configuration, users can use either one 16i adapter with onboard NVMe ports or two 8i adapters with onboard NVMe ports to support these backplanes.

A.

NVMe ports

One 16-port adapter with onboard NVMe ports

B.
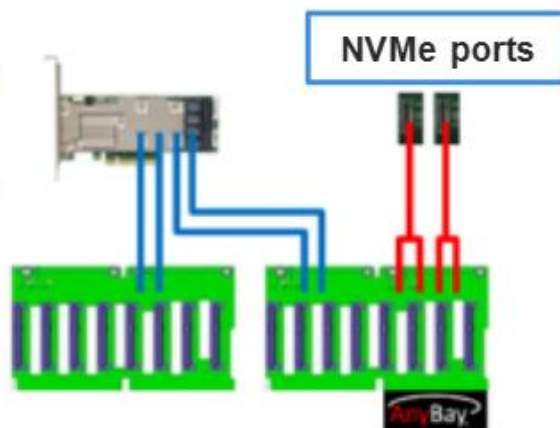
NVMe ports

Two eight-port adapters with onboard NVMe ports
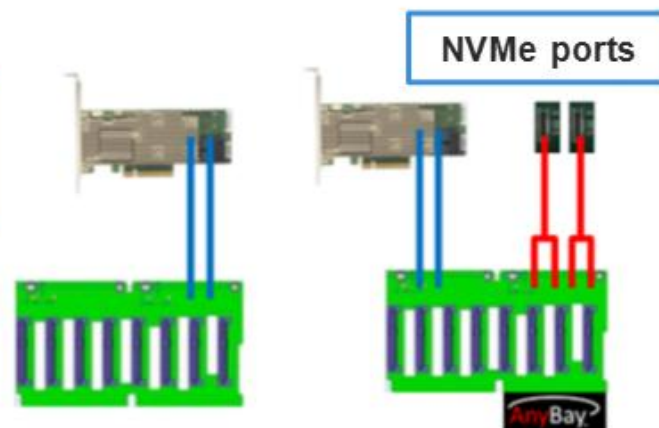
Sixteen drive bays, where eight are AnyBay bays – four processors

In this configuration, users can use either one 16i adapter with onboard NVMe ports or two 8i adapters with onboard NVMe ports to support these backplanes.

A.

One 16-port, one NVMe adapter, and onboard NVMe ports
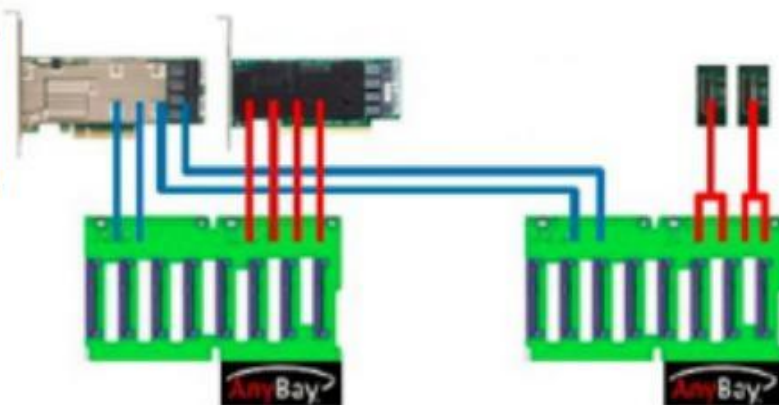
B.

Two eight-port, one NVMe adapter, and onboard NVMe ports
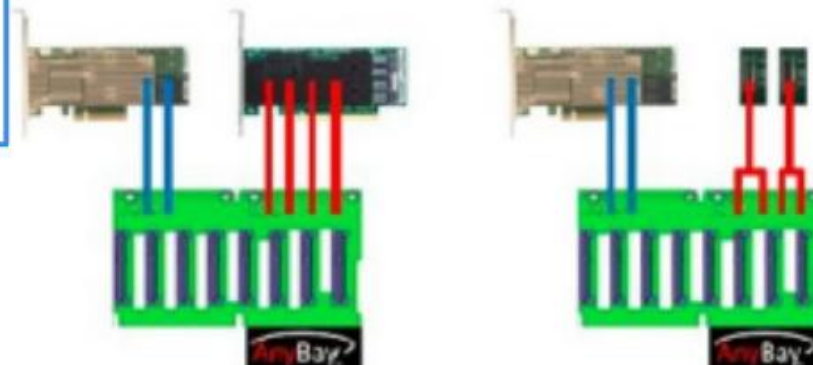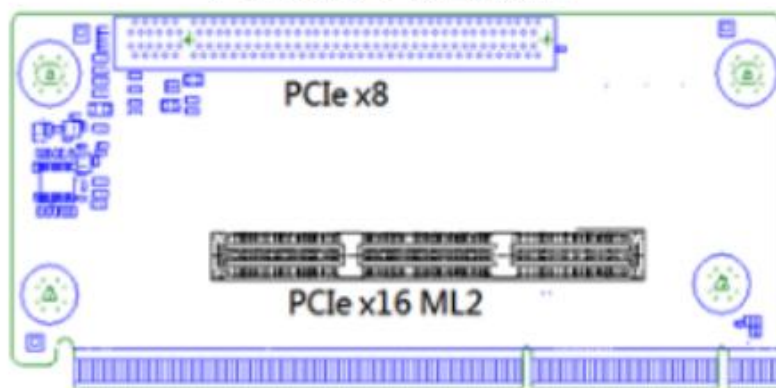
PCIe slots

The PCIe slots are as follows:
- Slot 1: PCIe 3.0 x16 (low profile) (CPU 2)
- Slot 2: PCIe 3.0 x8 (low profile) (CPU 2)
- Slot 3-5: Riser card slots (refer to PCIe riser options) (CPU 2)
- Slot 8: PCIe 3.0 x8 (low profile) (CPU 1)
- Slot 10: PCIe 3.0 x16 (low profile) (CPU 1)
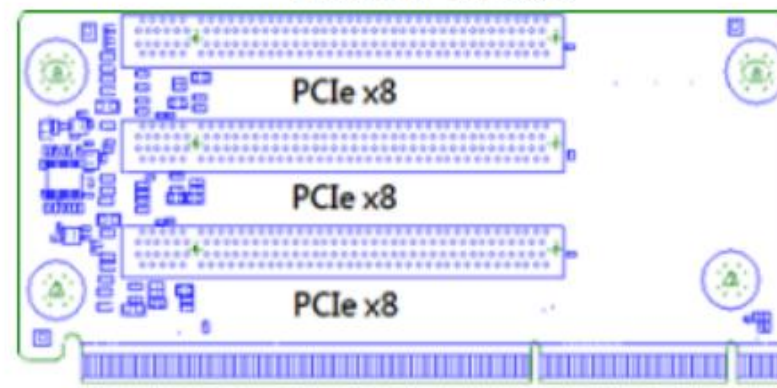- Slot 11: PCIe 3.0 x16 (low profile) (CPU 1)
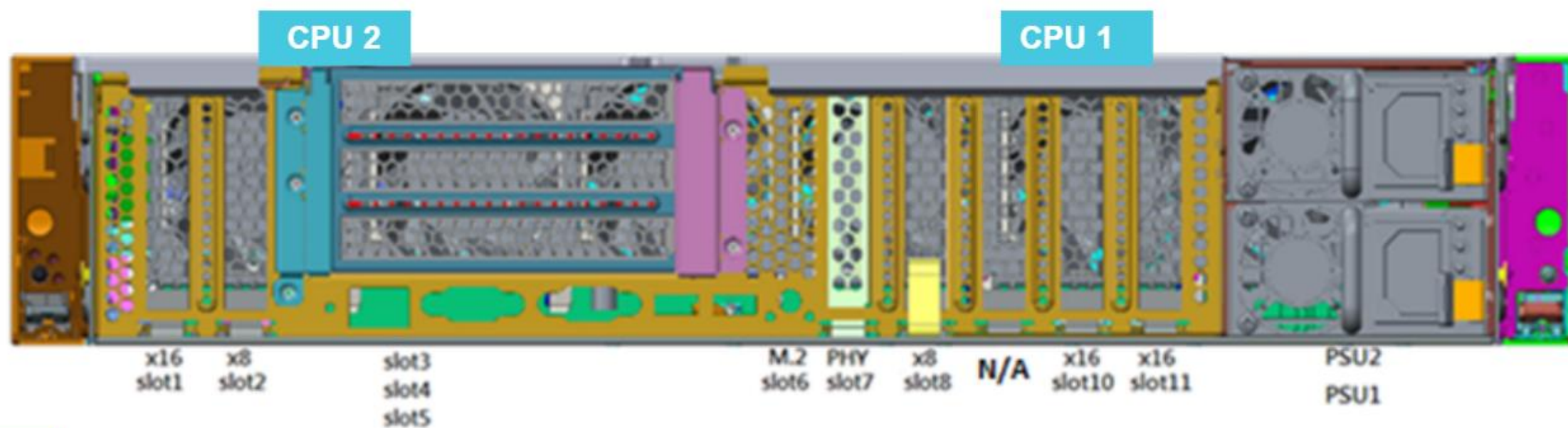
SR850P PCIe riser card options

There are four PCIe riser adapter options for the SR850P server. All slots (3, 4, 5) accept full-height half-length (FHHL) cards.
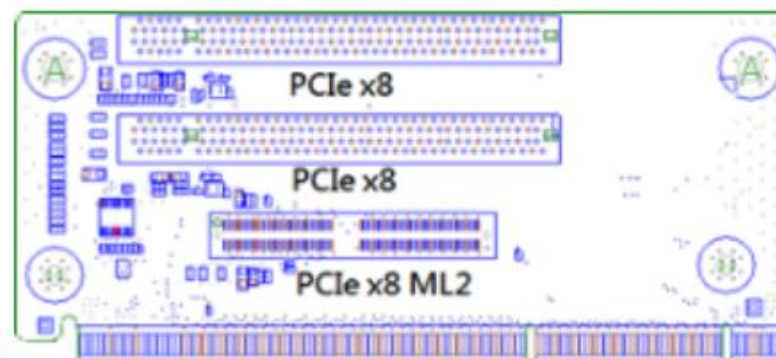

PCIe x8 + ML2 x16

PCIe x8

PCIe x16 ML2

Three PCIe x8

PCIe x8

PCIe x8

PCIe x8

Two PCIe x8 + ML2 x8

PCIe x8

PCIe x8

PCIe x8 ML2

PCIe x16 + PCIe x8

PCIe x16

PCIe x8