

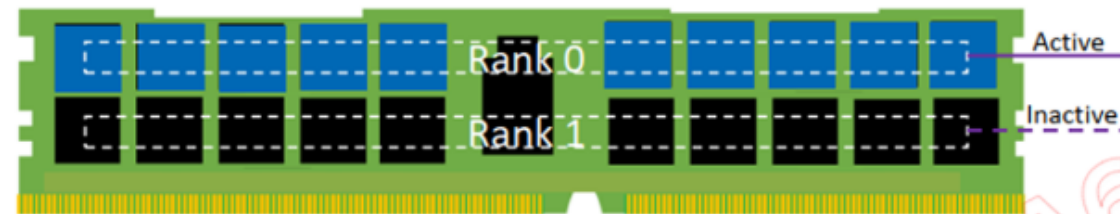
# Supported DIMMs

New memory modules supported with Intel Xeon 6 processors

Lenovo

## MRDIMM overview

Xeon 6 supports MRDIMMs. MRDIMMs (Multiplexed Rank Dual Inline Memory Modules) are an enhanced DDR5 DIMM technology that deliver 30% greater memory bandwidth than RDIMMs with an expected data transfer rate of up to 8800 MT/s. The MRDIMM is the fastest DDR5 DIMM currently available, and they are supported by Intel Xeon P-cores processors.



Dual Rank RDIMM – Only 1 rank is active during a R/W cycle based on CS

Each rank operates independently to achieve rated speed



Dual Rank MRDIMM – Two ranks operate simultaneously to combine data lines

using buffer chips located above edge fingers to achieve higher data rate

# Xeon 6 memory config

- Xeon 6900 P-cores processors support 1DPC (DIMM per channel) population only
- 6500 / 6700-series supports both 1DPC and 2DPC population
  - 2DPC population is only supported with RDIMMs, not with MRDIMMs
- MRDIMMs are supported only on P-cores processors with 1DPC population

DIMM rating	Operating speed (MT/s)	Memory config
Xeon 6900 P-cores		
DDR5-6400 rated RDIMMs only	6400, 6000, 5600, 5200, 4800	1DPC / 1SPC
MR-8800 only	8800, 8000, 7200	1DPC / 1SPC
Xeon 6500 / 6700 P-cores		
DDR5-6400 rated RDIMMs only	6400, 6000, 5600, 5200, 4800	1 DPC / 1 SPC
	5200, 4800	2 DPC / 2 SPC
MR-8800 only	5200, 4800	1 DPC / 1 SPC
Xeon 6700 E-cores		
DDR5-6400 rated RDIMMs only	6400, 6000, 5600, 5200, 4800	1 DPC / 2 SPC
	5200, 4800	2 DPC / 2 SPC
Xeon 6900 E-cores		
DDR5-6400 rated RDIMMs only	6400, 6000, 5600, 5200, 4800	1 DPC / 1 SPC

- DPC = DIMM per channel
- SPC = slot per channel

## CXL technology

ThinkSystem V4 servers support **Compute Express Link** (CXL) 2.0. CXL is an industry-supported **cache-coherent interconnect** for **processors**, **memory expansion**, and **accelerators**. For more information about **CXL technology**, refer to the following documentation:

- CXL organization: About CXL:

<https://computeexpresslink.org/about-cxl/>

- **Breaking the memory** wall with **compute express link** (CXL):

<https://community.intel.com/t5/Blogs/Tech-Innovation/Data-Center/Breaking-the-Memory-Wall-with-Compute-Express-Link-CXL/post/1594848>

