



Processor

Skylake processor features and configurations



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- The diagram illustrates the internal architecture of an Intel Xeon Scalable Processor, centered around a blue rounded rectangle representing the processor chip. At the top of the chip is the 'Fabric' block, which connects to the 'Integrated Fabric: Intel Omni-Path Architecture' box above. Below the fabric is the 'PCIe*3.0' and 'DMI' interface. The central 'System Agent' block is connected to 'IMC' (Integrated Memory Controller) blocks on either side, which in turn connect to memory channels (represented by green and yellow blocks). Below the System Agent is a stack of 'Core' and 'LLC' (Last Level Cache) blocks. At the bottom of the chip is the 'Intel UPI' (Ultra Path Interface) block. Surrounding the chip are various feature boxes, color-coded to indicate their status: green for existing features and blue for new Skylake server features. On the left, features include 14 nm process technology, PCI Express* 3.0 48 Lanes, Intel Hyper-Threading Technology (two threads/core), Intel Turbo Boost Technology, Up to 28 cores, and Integrated Voltage Regulator. On the right, features include Power Management (Per Core P-State (PCPS), Uncore Frequency Scaling (UFS), Energy Efficient Turbo (EET), On die PMAX detection (new), Intel® Speed Shift Technology (HWP) (NEW)), Memory Technology (6xDDR4 channels, 2133, 2400, 2666 MT/s, RDIMM, LRDIMM, Apache Pass), Rebalanced Cache Hierarchy (Increased MLC, 1.375 MB Last Level Cache/Core), Intel AVX-512, and Intel UPI. A legend at the bottom left identifies the color coding: blue for 'New Skylake server feature' and green for 'Existing feature'. The bottom of the slide mentions 'Socket B 3,647 pins'.
- Integrated Fabric:
Intel Omni-Path Architecture
- 14 nm process technology
- PCI Express* 3.0 48 Lanes
- Intel Hyper-Threading Technology (two threads/core)
- Intel Turbo Boost Technology
- Up to 28 cores
- Integrated Voltage Regulator
- Fabric
- PCIe*3.0 DMI
- IMC System Agent IMC
- Core LLC
- Core LLC
- Core LLC
- Core LLC
- Core LLC
- Core LLC
- Core LLC
- Core LLC
- Intel UPI
- Power Management:
Per Core P-State (PCPS)
Uncore Frequency Scaling (UFS)
Energy Efficient Turbo (EET)
On die PMAX detection (new)
Intel® Speed Shift Technology (HWP) (NEW)
- Memory Technology:
6xDDR4 channels
2133, 2400, 2666 MT/s
RDIMM, LRDIMM, Apache Pass
- Rebalanced Cache Hierarchy:
Increased MLC
1.375 MB Last Level Cache/Core
- Intel AVX-512
- Intel UPI
- New Skylake server feature
- Existing feature
- Socket B 3,647 pins

IMC represents integrated memory controller.

Socket P – 3,647 pins

Processor product numbering

The image explains processor numbering rules.



Processor levels and features

Four-socket supported processors

This is a feature comparison table of the processor scalable family.

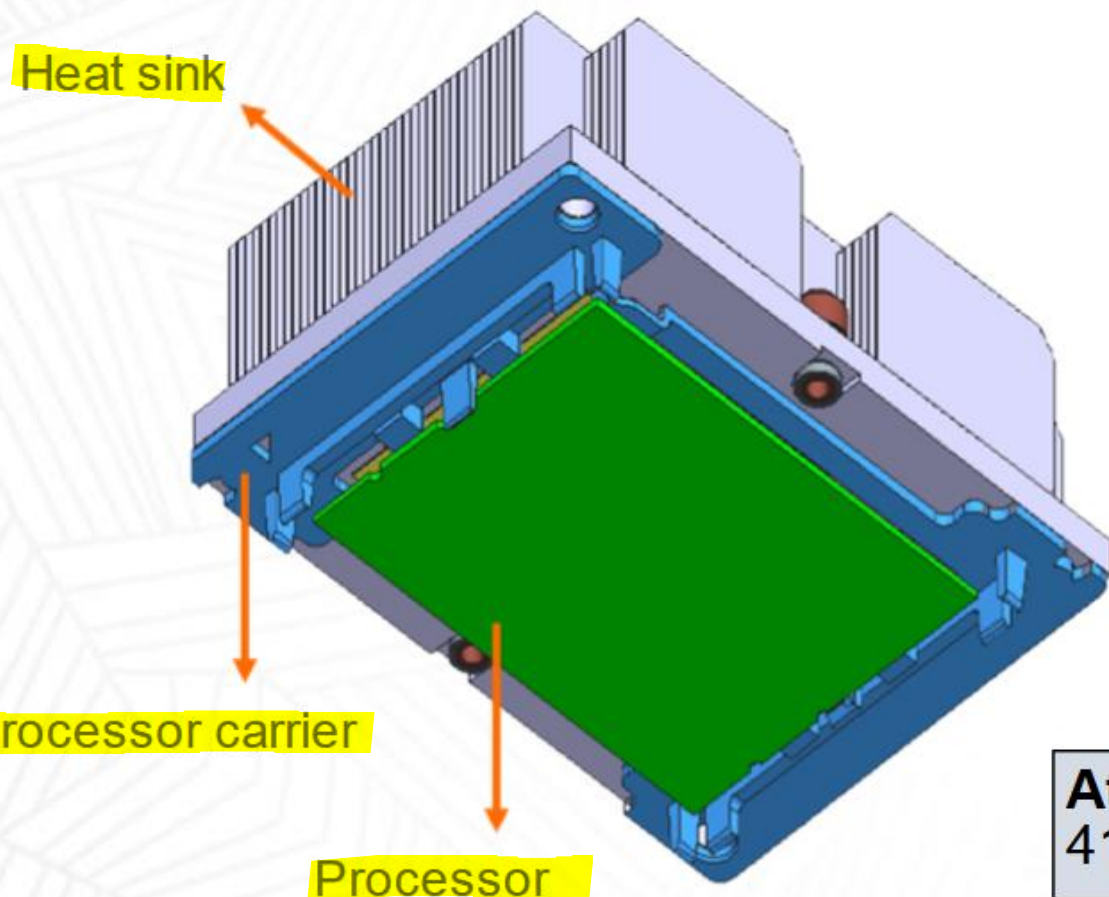
Feature	81xx (Platinum)	61xx (Gold)	51xx (Gold)	41xx (Silver)	31xx (Bronze)
Number of Intel UPI links	Three	Three	Two	Two	Two
UPI speed	10.4 GT/s	10.4 GT/s	10.4 GT/s	9.6 GT/s	9.6 GT/s
Supported topologies	3 UPI → 2S-2UPI, 2S-3UPI, 4S-2UPI, 4S-3UPI, 8S-3UPI	3 UPI → 2S-2UPI, 2S-3UPI, 4S-2UPI, 4S-3UPI	2S-2UPI, 4S-2UPI	2S-2UPI	2S-2UPI
Node controller support	Yes	Yes	No	No	No
Number of memory channels	Six	Six	Six	Six	Six
DDR4 speed	2666	2666	2400*	2400	2133
Memory capacity	768 GB, 1.5 TB (select SKUs**)	768 GB, 1.5 TB (select SKUs**)	768 GB	768 GB	768 GB
RAS capability	Advanced	Advanced	Advanced	Standard	Standard
Intel Turbo Boost Technology	Yes	Yes	Yes	Yes	No
Inter Hyper-Threading Technology	Yes	Yes	Yes	Yes	No
Intel AVX-512 ISA support	Yes	Yes	Yes	Yes	Yes
Intel AVX-512 – # of 512b FMA units	Two	Two	One*	One	One
Number of PCIe lanes	48	48	48	48	48

* Gold processor #5122 supports 2666 DDR4 and two 512-bit FMA units.

** SKUs that support 1.5 TB per socket memory capacity are shown [here](#).

Processor heat sink module

The **processor heat sink module** (PHM) refers to the subassembly where the **heat sink** and **processor** are **clipped together** prior to installation.



Click CPU FRUs and PHM assembly to view the details.

SKX standard

SKX-F

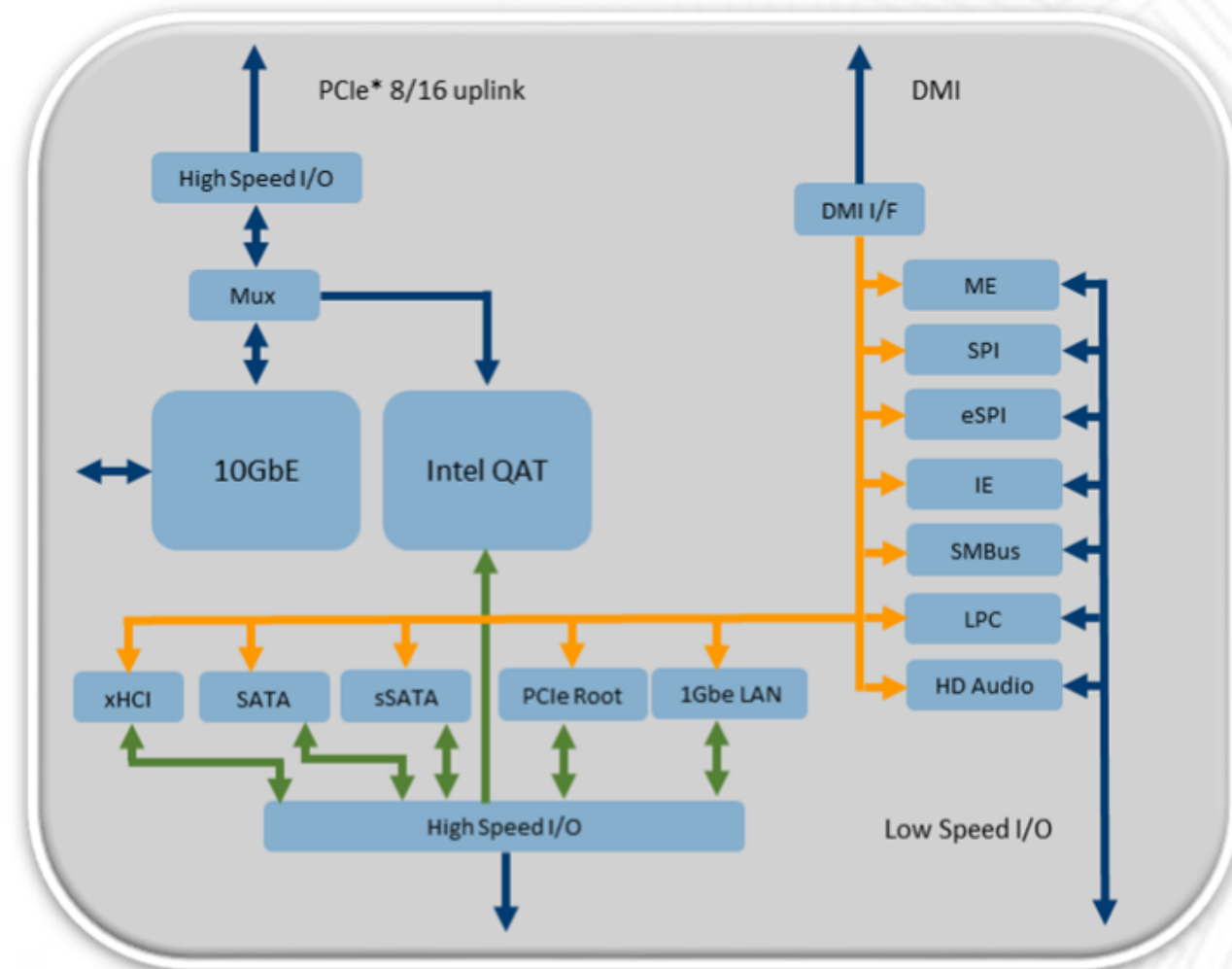
PHM to system board assembly

Attention: Use the **gray thermal grease** (part number 41Y9292) when replacing the processor.

Intel C620 series chipsets Southbridge (Lewisburg PCH)

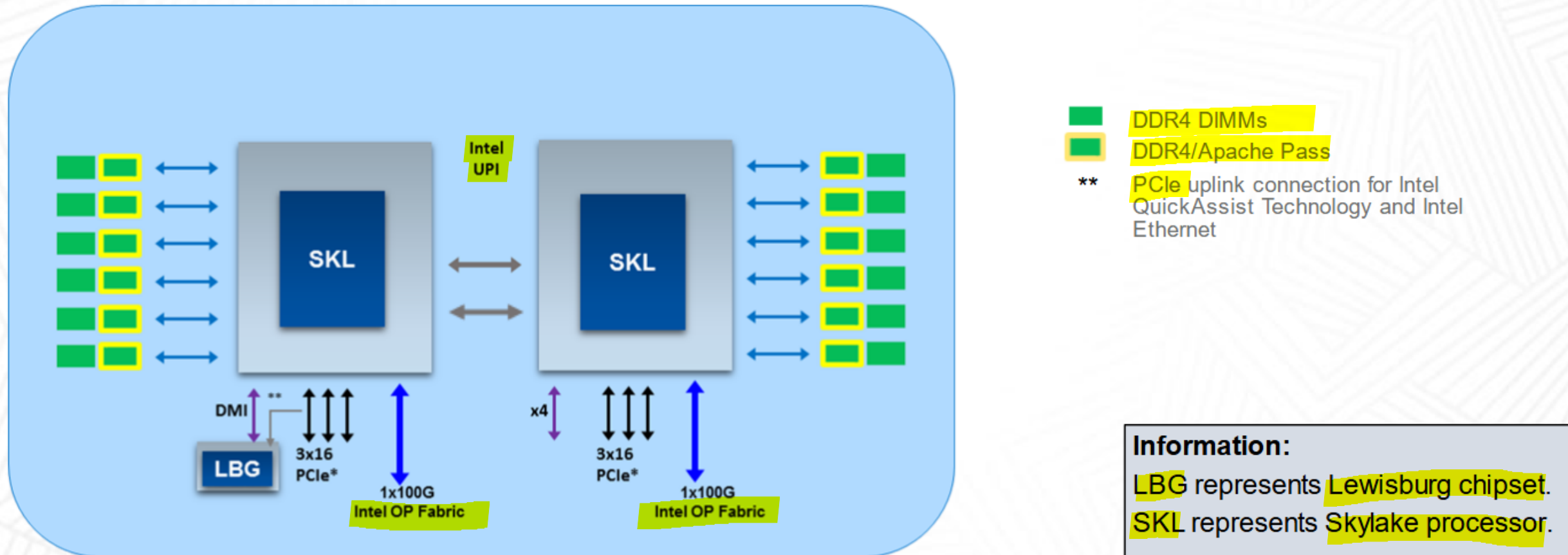
Intel Xeon scalable processors with Intel C620 series chipsets deliver new levels of consistent performance. Here are the key features of Intel C620 series chipsets:

- Integrated Intel X722 Ethernet, up to Quad 10 Gbit (x8 uplink)
- Node Manager 4.0
- Direct media interface (DMI) x4 link is now Gen3, supporting up to 8 Gbit
- ThinkSystem servers use enhanced serial peripheral interface (eSPI) and not lower pin count (LPC) interface



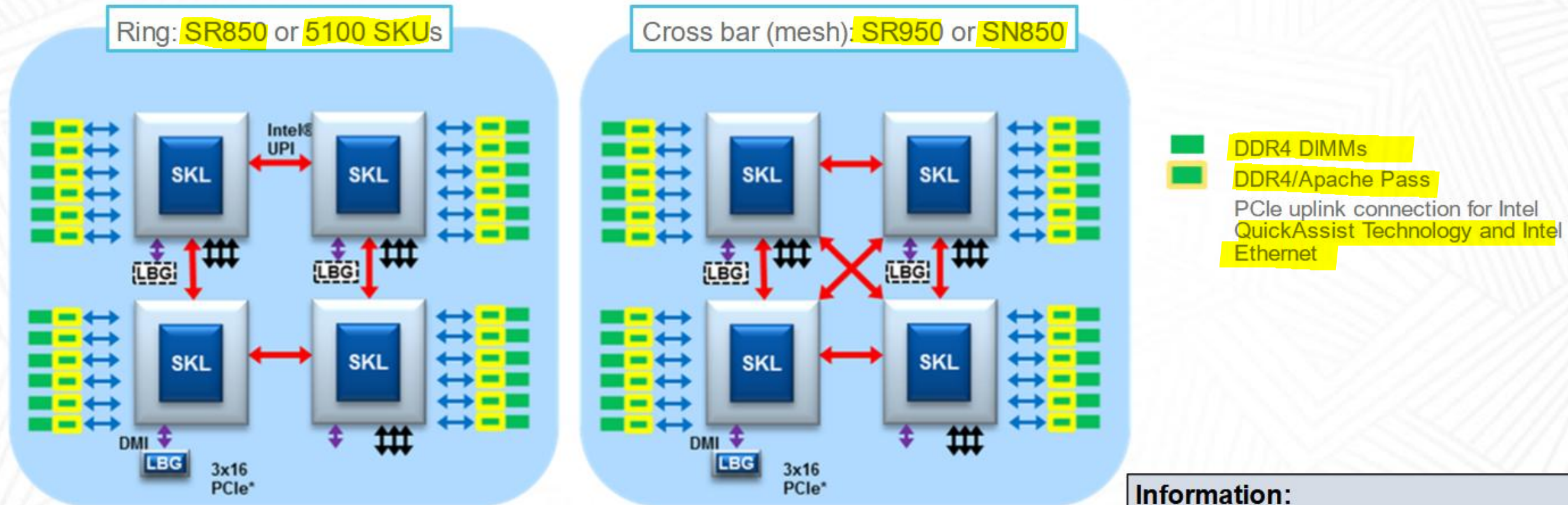
Typical 2S-2UPI configuration

This graphic shows **two-socket platform** configuration. In this example, a DIMM population is shown. Look up **Apache Pass** customer collateral for specific rules on **DDR4/Apache Pass DIMM populations**.



Typical 4S configuration

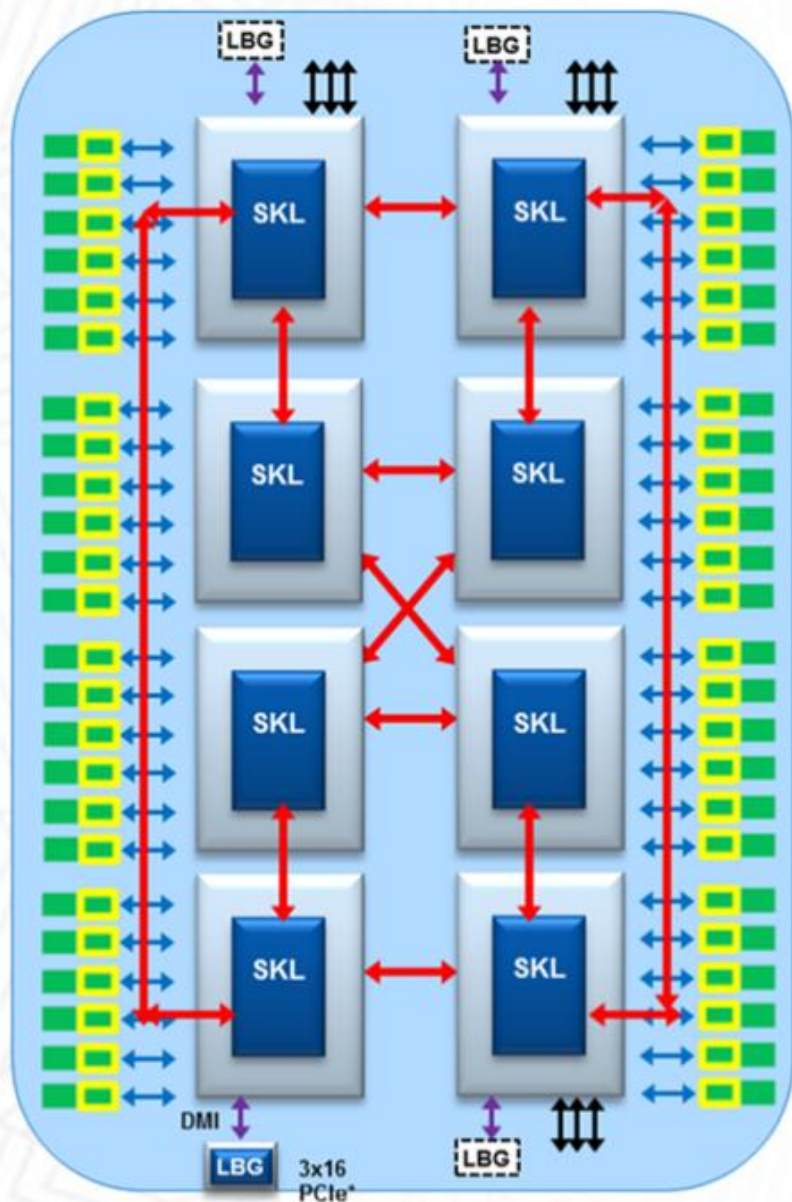
This graphic shows four-socket platform configuration.



Information:

LBG represents Lewisburg chipset.
SKL represents Skylake processor.

Typical 8S configuration (SR950)



This graphic shows eight-socket platform configuration.

- DDR4 DIMMs
- DDR4/Apache Pass
- LBG Optional
PCIe uplink connection for Intel
QuickAssist Technology and Intel Ethernet

Information:

LBG represents Lewisburg chipset.

SKL represents Skylake processor.



RAS features

RAS features on 5100/6100/8100 SKUs



High-value RAS features on 5100/6100/8100 SKUs

- Adaptive Double Device Data Correction with Multiple Regions (ADDDC-MR) (Memory Self-Healing)
 - Requires two ranks of x4 DIMMs per DDR4 channel for best MR features.
 - Requires closed-page memory.
- Machine Check Architecture
 - Recovery for a limited set of faults
 - Error containment for improved reporting and isolation
- UPI Faildown (link width reduction, but server keeps running)
 - Link can retrain from 20 data lanes to eight data lanes
- Address Based Mirroring (6 GB per CPU when the option is selected)
 - Provides RAID1 protection on critical areas of memory like OS or Hypervisor

Note: Use Adaptive open-page if maximum performance mode is needed. However, you will not get full RAS capability while in maximum performance mode.